EAST EUROPEAN JOURNAL OF PHYSICS. 2. 275-279 (2026)
DOI:10.26565/2312-4334-2026-2-29 ISSN 2312-4334

RESISTIVE SWITCHING BEHAVIOR OF Si/TiO THIN FILMS FOR NON-VOLATILE MEMORY APPLICATIONS

Muradulla T. Normurodov[1], Odil Ochilov[2], Ozodbek Y. Yuldashev[2]*, Zarnigor A. Karshieva[2], Nurbek U. Toshboyev[2]
[1]*Karshi State University, Uzbekistan*
[2]*Center of Nanotechnology Development, National University of Uzbekistan, Tashkent, Uzbekistan*
**Corresponding Author e-mail: ozodbekyoldoshev997@gmail.com*
Received December 16, 2025; revised March 26, 2026; accepted April 1, 2026

This study presents the fabrication of Si/TiO thin films deposited in DC mode via magnetron sputtering onto p-type silicon substrates and investigates their temperature-dependent resistive switching (RS) and low-resistance state (LRS) characteristics. The nanostructures were annealed at 420°C to improve crystallinity and interfacial contact. Electrical characterization through I–V measurements revealed clear bipolar RS behavior without the need for an initial forming process. The devices exhibited stable high-resistance (HRS) and low-resistance (LRS) states over multiple cycles. The switching mechanism is explained by the formation and rupture of conductive filaments induced by oxygen vacancies at the Si/TiO interface. Bandgap values obtained from Tauc plots were approximately 3.24 eV for TiO and 3.41 eV for SnO_2. These results confirm that Si/TiO nanothin films are promising materials for next-generation fast, energy-efficient, and rewritable memory devices.
Keywords: *TiO; Magnetron Sputtering; Memristor; Rapid Thermal Annealing (RTA)*
PACS: 85.50-n

INTRODUCTION

In recent years, memristors have emerged as one of the most dynamic and influential research directions, driven by their promising applications in neuromorphic computing, advanced artificial intelligence hardware, and next-generation non-volatile memory technologies. Recognized as the fourth fundamental passive circuit element—alongside resistors, capacitors, and inductors—memristors uniquely possess the ability to retain a memory of their resistance state based on the prior flow of electrical charge. This intrinsic memory effect enables them to store information even without external power, positioning memristors as highly attractive candidates for low-power, high-density memory architectures.

Among the various material platforms, metal-oxide-based memristors—particularly those employing binary oxides such as TiO and SnO_2—have gained substantial attention due to their low fabrication cost, straightforward synthesis routes, and excellent compatibility with flexible electronic substrates. Both TiO and SnO_2 are wide-bandgap n-type semiconductors, with bandgap energies of approximately 3.4 eV and 3.6 eV, respectively. TiO is known for its high electron mobility and pronounced surface reactivity, whereas SnO_2 demonstrates remarkable chemical stability and exhibits enhanced electrical conductivity when appropriately doped [4,5]. When these oxides are engineered into nanolayered or nanostructured forms, they can exhibit additional resistive switching pathways, including interface-controlled filament formation and oxygen-vacancy-driven migration processes.

Pant et al. [6] reported pronounced bipolar resistive switching and clearly defined negative differential resistance (NDR) behavior in Si/TiO nanostructures synthesized via magnetron sputtering. These features were attributed to enhanced grain-boundary diffusion and quantum confinement effects at nanoscale interfaces. More recently, Saha and co-workers [7] demonstrated reliable, sharply defined switching characteristics in one-dimensional TiO nanofiber-based memristors, revealing that artificial neural networks (ANN) can accurately model and predict switching dynamics. Additionally, the NDR behavior observed in Co-doped SnO_2 memristors deposited on p-type silicon substrates highlights the profound influence of dopants on the electronic properties of oxide nanostructures [8]. In the present work, we examine the resistive-switching characteristics of a p-Si/TiO nanofilm fabricated by magnetron sputtering (MS). The TiO layers were sequentially deposited onto p-type silicon and quartz substrates and subsequently annealed at 420 °C. Current–voltage (I–V) measurements performed with a Keithley 2460 SourceMeter revealed a distinct hysteresis loop characteristic of memristive behavior. However, due to the close similarity in the bandgap energies of TiO and SnO_2, the resulting switching contrast may be relatively limited, as both oxide layers tend to exhibit p-type semiconductor characteristics. Overall, this study contributes to ongoing efforts to optimize binary oxide nanostructures for implementation in low-power, non-volatile memory devices

METHODS

Thin nanostructured p-Si/TiO films were fabricated using the magnetron sputtering (MS) technique. This method is known for its low cost, convenience, and high suitability for oxide film formation. In this study, p-type silicon substrates

Cite as: M.T. Normurodov, O. Ochilov, O.Y. Yuldashev, Z.A. Karshieva, N.U. Toshboyev, East Eur. J. Phys. 2, 275 (2026), https://doi.org/10.26565/2312-4334-2026-2-29

were used. Prior to deposition, the substrates were sequentially cleaned by rinsing in deionized (DI) water, followed by ethanol and acetone, and then rinsed again in DI water. Additionally, they were treated with argon plasma inside the magnetron sputtering system. This multistep cleaning procedure was carried out to completely remove inorganic and organic contaminants and to ensure uniform film formation with good adhesion. After cleaning, the substrates were dried in a nitrogen flow and kept under vacuum in the magnetron sputtering system.

The schematic structure of the fabricated memristor device is shown in Figure 1. The device consists of a p-Si/TiO nanostructure deposited on a p-type silicon substrate. Tin oxide (SnO_2) contacts were used as the top electrode. The TiO layer serves as an intermediate interface layer, while SnO_2 acts as the top oxide electrode, and the p-Si substrate functions as the bottom electrode. This vertical "sandwich-like" configuration enables charge transport through the oxide layers under an applied electric field and allows investigation of resistive switching behavior.

The applied multistep cleaning procedure reduces surface contamination, thereby promoting the formation of uniform films with good adhesion and, consequently, improving the stability and reproducibility of the electrical characteristics of the memristor devices [9].

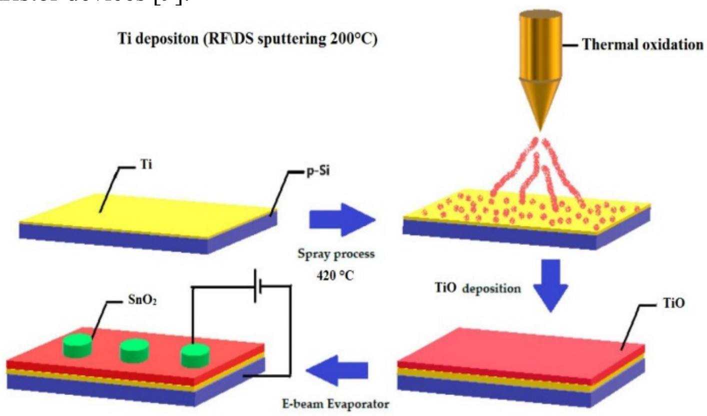

Figure 1. Schematic illustration of the SnO_2/TiO/p-Si memristor device structure

To obtain the SnO_2 electrodes, a contact pattern was created using a mask in the magnetron sputtering system, with oxygen gas as the carrier gas directed toward the heated substrate.

The deposition process was carried out at a temperature of 420°C, monitored using a controlled display. The TiO layer was deposited first, followed by the SnO_2 electrode through a mask to form the nanostructure. This sequence was chosen to ensure proper band alignment and good interfacial contact between the n-type semiconductors. After deposition, the films were annealed at 420°C with oxygen flow to enhance crystallinity and stabilize the interface. For electrical measurements, tin oxide (SnO_2) contacts were applied, and the p-Si substrate served as the bottom electrode electrical characterization of the memristor devices was performed using a Keithley 2460 SourceMeter. A voltage sweeps sequence of 0 → +3 V → 0 → –3 V → 0 was applied to investigate the current–voltage (I–V) characteristics. The hysteresis loop observed in the I–V curve confirmed the presence of resistive switching behavior in the fabricated structures transducer and carried toward the heated substrates using oxygen gas as the carrier.

The deposition process was conducted at a substrate temperature of 450 °C, which was maintained using a controlled hotplate. The SnO_2 was deposited first, followed by the ZnO layer, forming a bilayer heterostructure. This sequence was designed to promote appropriate band alignment and interfacial contact between the n-type semiconductors. Following deposition, the films were annealed in ambient air at 450 °C to improve crystallinity and stabilize the interface. Silver (Ag) top contacts were applied using silver paste for electrical measurements, and the p-Si substrate served as the bottom electrode in the case of silicon-based structures.

Electrical characterization of the memristor devices was performed using a Keithley 2460 SourceMeter. A voltage sweeps protocol of 0 → +3 V → 0 → –3 V → 0 was applied to examine the current–voltage (I–V) characteristics. The presence of a hysteresis loop in the I–V curve confirmed the resistive switching behavior of the fabricated structures.

RESULTS

A. Current–Voltage (I–V) Characteristics

The I–V characteristics of TiO thin films treated in air by Rapid Thermal Annealing (RTA) at 500°C, 600°C, 700°C, 800°C, and 900°C for 10 minutes are shown. It was observed that the memristive behavior of the TiO thin films improved as the annealing temperature increased. To initiate the formation of a conduction path in the metal oxide, the forming voltage was set to 3 V. Bipolar resistive switching behavior was observed for these samples.

Initially, the current increased linearly with voltage according to Ohm's law, then entered a quasi-saturation region. This quasi-saturation stage is explained by the space-charge-limited conduction (SCLC) mechanism, in which charge carriers experience delayed transport [11]. Subsequently, the current increased abruptly, showing a rapid transition from the high-resistance state (HRS) to the low-resistance state (LRS). This sudden increase in current is associated with the formation of conductive filaments (CFs) in TiO induced by oxygen vacancies. Well-defined memory windows were

observed for the samples annealed at higher temperatures (up to 900°C). Kars *et al.* [7] reported that the formation of oxygen vacancies during low-temperature annealing is related to the breaking of Ti–O bonds.
At the same time, atmospheric oxygen attaches to the surface of the TiO film, forming Ti–O bonds [2]. Thus, there is a competition between the breaking of Ti–O bonds in the bulk and the formation of Ti–O bonds at the surface.

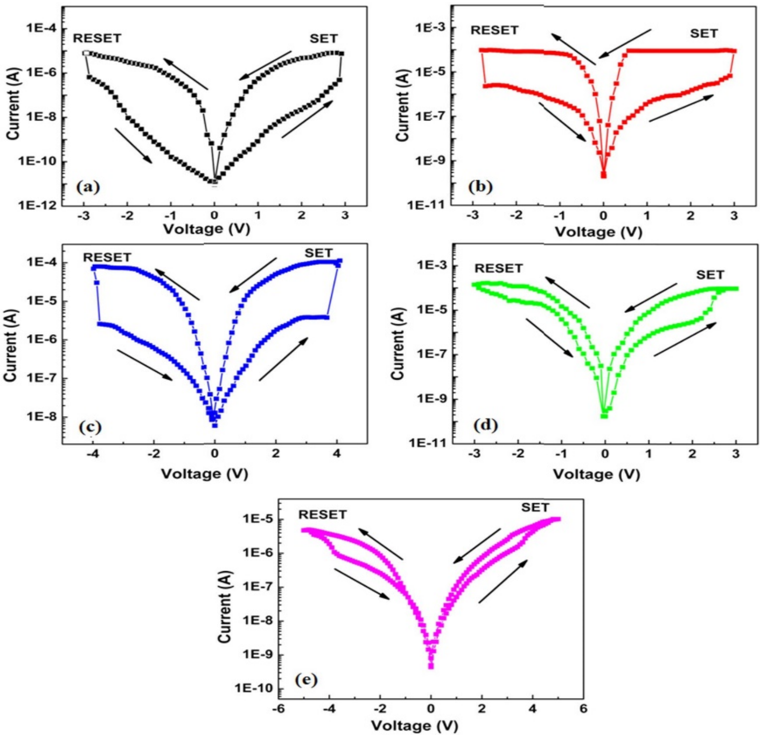

Figure 2. I–V curves of dip-coated TiO thin films processed for 10 min in air ambient with various Rapid Thermal Annealing (RTA) a) 500°C, b) 600°C, c) 700°C, d) 800°C, and e) 900°C

B. Optical Bandgap Estimation

The optical bandgaps of the individual TiO and SnO_2 layers were estimated using Tauc plot analysis derived from UV–Vis absorbance spectra (see Figure 3). By plotting $(\alpha h\nu)^2$ versus photon energy ($h\nu$) and extrapolating the linear region to the energy axis, the direct bandgap values were determined. The estimated optical bandgaps were found to be approximately: TiO layer (3.17 eV), SnO_2 layer (3.41 eV)

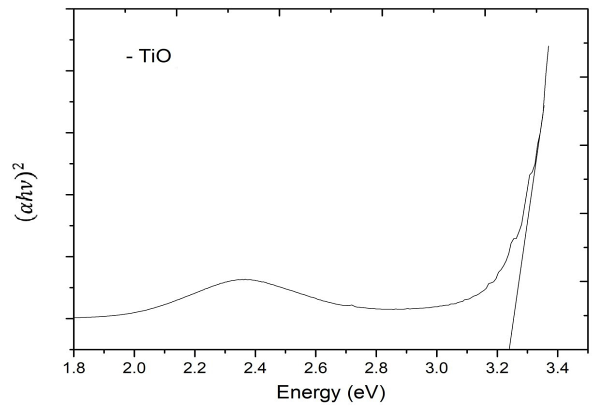

Figure 3. Tauc plot used for bandgap estimation of TiO (3.24 eV)

These values closely match literature-reported data confirming the successful synthesis of phase-pure oxide layers. The slight narrowing of the SnO_2 bandgap compared to the nominal 3.6 eV may be attributed to oxygen vacancy-related subgap states, which can affect the switching performance by serving as electron trapping centers.

C. Structural Characterization (XRD analysis)

Figure 4 shows the XRD patterns of TiO thin nanoplanes processed in air at 500 °C for different durations (1, 5, and 10 min). The XRD peaks at 26.7° and 49.1° correspond to the (101) and (200) planes of the anatase phase, respectively, which are consistent with literature reports. The intensity of the (101) peak decreases with increasing annealing duration.

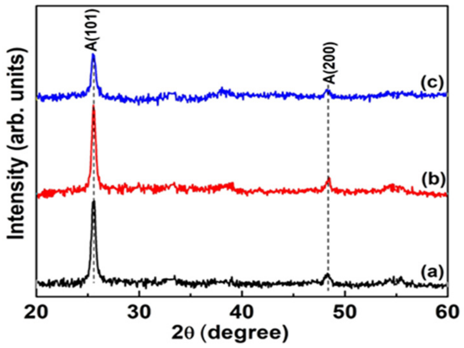

Figure 4. XRD patterns of dip-coated TiO thin films processed at 500°C in air ambient for different RTA duration a) 1min, b) 5min, and c) 10min (the abbreviation stands for: A anatase)

D. Mechanism Interpretation

To identify the charge transport mechanism in the TiO layer for the LRS (Low Resistance State) and HRS (High Resistance State), we monitored the temperature dependence of the electrical conductivity in both states. These results are presented in Figure 5, where the thermally activated behavior of the LRS and HRS within the TiO layer is clearly visible.

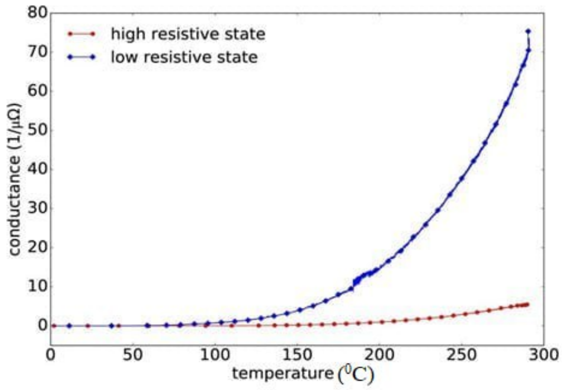

Figure 5. To determine the charge transport mechanism in the LRS and HRS states of the TiO layer, we monitored the temperature dependence of the conductivity in both states. This is shown in the figure, where the thermally activated behavior of the LRS and HRS within the TiO layer is clearly visible

CONCLUSIONS

In this study, a p-Si/TiO thin film was successfully fabricated using the magnetron sputtering technique. Electrical analysis of the device revealed clear bipolar resistive switching behavior accompanied by a stable hysteresis loop in the I–V characteristics. The fact that the switching occurred without the need for a forming step indicates that oxygen vacancies and interface effects play a major role in the resistive switching (RS) mechanism. Tauc plot analysis showed that the optical bandgaps of TiO and SnO_2 were approximately 3.24 eV and 3.41 eV, respectively, which are consistent with values reported in the scientific literature. Although both oxides are n-type semiconductors and the small band offset between them may slightly reduce the overall switching contrast, the device exhibited repeatable SET/RESET cycles and sufficient separation between the resistance states.

These results confirm that the p-Si/TiO nanostructure is a promising platform for exploring low-cost, oxide-based memristors. Future studies may focus on interface engineering, doping, or incorporating buffer layers to further enhance RS characteristics and improve device scalability for neuromorphic and non-volatile memory applications.

ORCID

Muradulla X. Normurodov, https://orcid.org/0000-0003-1771-0853; **Odil O. Ochilov,** https://orcid.org/0000-0002-9319-0143; **Ozodbek Y. Yuldashev**, https://orcid.org/0009-0000-6464-3484; **Zarnigor A. Karshieva,** https://orcid.org/0009-0005-3837-538X; **Nurbek U. Toshboyev,** https://orcid.org/0009-0008-0057-5433

REFERENCES

[1] D. Ielmini, "Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling," Semiconductor Science and Technology, **31**(6), 063002 (2016). https://doi.org/10.1088/0268-1242/31/6/063002

[2] B. Cao, H. Liu, T. Li, J. Gong, S. Zhang, and M.T. Dove, "Synthesis of composite films for ZnO-based memristors with superior stability," Materials Research Express, **11**, 056302 (2024). https://doi.org/10.1088/2053-1591/ad4777

[3] P.D. Walke, *et al.*, "Memristive Devices from CuO Nanoparticles," Nanomaterials, **10**(9), 1677 (2020). https://doi.org/10.3390/nano10091677

[4] P.A. Hind, P. Kumar, U.K. Goutam, and B.V. Rajendra, "Impact of deposition temperature on persistent photoconductivity of SnO_2 thin films deposited using spray pyrolysis technique suitable in optoelectronic synaptic devices," Optical Materials, **146**, 115579 (2024). https://doi.org/10.1016/j.optmat.2024.115579
[5] N.U. Rehman, R. Khan, N. Rahman, I. Ahmad, A. Ullah, M. Sohail, S. Iqbal, et al., "Dual-doped ZnO-based magnetic semiconductor resistive switching response for memristor-based technologies," Journal of Materials Science: Materials in Electronics, **35**, 1557 (2024). https://doi.org/10.1007/s10854-024-13318-5
[6] R. Pant, N. Patel, K.K. Nanda, and S.B. Krupanidhi, "Negative differential resistance and resistive switching in SnO_2/ZnO interface," Journal of Applied Physics, **122**(12), (2017). https://doi.org/10.1063/1.5004969
[7] I. Kars, S.Ş. Çetin, B. Kinaci, B. Sarikavak, A. Bengi, H. Altuntaş, M.K. Öztürk, and S. Özçelik, "Influence of thermal annealing onthe structure and optical properties of d.c. magnetron sputteredtitanium dioxide thin films," Surf Interface Anal. **42**, 1247-1251 (2010). https://doi.org/10.1002/sia.3373
[8] S. Saha, *et al*. "Experimental demonstration of SnO_2 nanofiber-based memristors and their data-driven modeling for nanoelectronic applications," Chip, **2**, 100075 (2023). https://doi.org/10.1016/j.chip.2023.100075
[9] J.X. Murodov, Sh.U. Yuldashev, M.S. Mirkamilova, and U.E. Jurayev, "Tunable Negative Differential Resistance in SnO_2:Co Memristors on p-Si," East European Journal of Physics, (2), 211-214 (2025). https://doi.org/10.26565/2312-4334-2025-2-22
[10] A. Arslanov, Sh. Yuldashev, N. Botirova, R. Nusretov, J. Murodov, and J. Xudoyqulov, "Impact of precursor molar concentration on the structural and optical properties of ZnO thin films synthesized by ultrasonic spray pyrolysis," Physical Science International Journal, **29**(1), 29–35 (2025). https://doi.org/10.9734/psij/2025/v29i1871
[11] P. Chowdhury, H.C. Barshilia, N. Selvakumar, B. Deepthi, K.S. Rajam, A.R. Chaudhuri, and S.B. Krupanidhi, "The structural and electrical properties of TiO2 thin films prepared by thermal oxidation," Phys. B Condens. Matter. **403**, 3718–3723 (2008). https://doi.org/10.1016/j.physb.2008.06.02
[12] D. Regonini, V. Adamaki, C.R. Bowen, S.R. Pennock, J. Taylor, and A.C.E. Dent, "AC electrical properties of TiO_2 and Magnéli phases, $TinO_{2n-1}$," Solid State Ionics, **229**, 38–44 (2012). https://doi.org/10.1016/j.ssi.2012.10.003
[13] Y. Le Page, and P. Strobel, "Structural chemistry of the Magnéli phases $TinO_{2n-1}$, $4 \leq n \leq 9$. II. Refinements and structural discussion," J. Solid State Chem. **44**, 273–281 (1982). https://doi.org/10.1016/0022-4596(82)90374-7
[14] L. Liborio, and N. Harrison, "Thermodynamics of oxygen-defective Magnéli phases in rutile: a first-principles study," Phys. Rev. B, **77**, 1–10 (2008). https://doi.org/10.1103/PhysRevB.77.104104
[15] Y. Abbas, I.S. Han, A.S. Sokolov, Y.R. Jeon, and C. Choi, "Rapid thermal annealing on the atomic layer-deposited zirconia thin filmto enhance resistive switching characteristics," J. Mater. Sci. Mater. Electron. **31**, 903–909 (2020). https://doi.org/10.1007/s10854-019-02598-x
[16] X.Y. Yang, Y.K. Zhu, H. Miura, and T. Sakai, "Static recrystallization behavior of hot-deformed magnesium alloy AZ31 during isothermal annealing," Trans. Nonferrous Met. Soc. China. **20**, 1269–1274 (2010). https://doi.org/10.1016/S1003-6326(09)60289-2
[17] M. Tian, M. Mahjouri-Samani, K. Wang, A.A. Puretzky, D.B. Geohegan, W.D. Tennyson, N. Cross, *et al*., "Black anatase formation by annealing of amorphous nanoparticles and the role of the Ti_2O_3 shell in self-organized crystallization by particle attachment," ACS Appl Mater. Interfaces, **9**, 22018–22025 (2017). https://doi.org/10.1021/acsami.7b02764
[18] Z.N. Jameel, A.J. Haider, and S.Y. Taha, "Synthesis of TiO_2 nanoparticles by using sol-gel method and its applications as antibacterial agents," Eng. Tech. J. **32**, 418–426 (2014). https://doi.org/10.30684/etj.32.3B.4
[19] N. Gergel-Hackett, B. Hamadani, B. Dunlap, J. Suehle, S. Member, C. Richter, S. Member, *et al*., "A flexible solution-processed memristor," IEEE Electron Device Lett. **30**, 706–708 (2009). https://doi.org/10.1109/LED.2009.202141
[20] K.N. Pham, V.D. Hoang, C.V. Tran, and B.T. Phan, "TiO_2 thin filmbased transparent flexible resistive switching random access memory," Adv. Nat. Sci. Nanosci. Nanotechnol. **7**, (2016). https://doi.org/10.1088/2043-6262/7/1/015017
[21] C. Ye, T. Deng, J. Zhang, L. Shen, P. He, W. Wei, and H. Wang, "Enhanced resistive switching performance for bilayer HfO_2/TiO_2resistive random access memory," Semicond. Sci. Technol. **31**, 1–7 (2016). https://doi.org/10.1088/0268-1242/31/10/105005
[22] C.H. Huang, T.S. Chou, J.S. Huang, S.M. Lin, and Y.L. Chueh, "Self-selecting resistive switching scheme using TiO_2 nanorod arrays," Sci. Rep. **7**, 1–9 (2017). https://doi.org/10.1038/s41598-017-01354-7

РЕЗИСТИВНА ПОВЕДІНКА ПЕРЕМИКАННЯ ТОНКИХ ПЛІВОК Si/TiO ДЛЯ ЗАСТОСУВАННЯ ЕЛЕКТРОНЕЗАЛЕЖНОЇ ПАМ'ЯТІ

Мурадулла Т. Нормуродов[1], Оділ Очілов[2], Озодбек Ю. Юлдашев[2], Зарнігор А. Каршієва[2], Нурбек У. Тошбоєв[2]
[1]*Каршинський державний університет, Узбекистан*
[2]*Центр розвитку нанотехнологій, Національний університет Узбекистану, Ташкент, Узбекистан*

У цьому дослідженні представлено виготовлення тонких плівок Si/TiO, нанесених у режимі постійного струму за допомогою магнетронного напилення на кремнієві підкладки p-типу, а також досліджено їх температурно-залежні характеристики резистивного перемикання (RS) та низькоомного стану (LRS). Наноструктури були відпалені при 420°C для покращення кристалічності та міжфазного контакту. Електрична характеристика, отримана за допомогою вольт-амперних вимірювань, виявила чітку біполярну поведінку RS без необхідності початкового процесу формування. Пристрої демонстрували стабільні стани високого (HRS) та низького (LRS) опору протягом кількох циклів. Механізм перемикання пояснюється утворенням і розривом провідних ниток, індукованих вакансіями кисню на межі розділу Si/TiO. Значення ширини забороненої зони, отримані з графіків Тауца, становили приблизно 3,24 еВ для TiO та 3,41 еВ для SnO_2. Ці результати підтверджують, що нанотонкі плівки Si/TiO є перспективними матеріалами для швидких, енергоефективних і перезаписуваних пристроїв пам'яті наступного покоління.

Ключові слова: *TiO; магнетронне розпилення; мемристор; швидкий термічний відпал (RTA)*