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ELECTROTHERMAL MODELING OF SELF-HEATING IN Si/GaAs p–n HETEROJUNCTIONS

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This study develops a coupled electrothermal model for predicting self-heating, heat transport, and temperature-dependent junction behavior in Si/GaAs p–n heterojunctions under high-power operating conditions.The model couples electrical and thermal processes to investigate the influence of Joule heating, thermal conductivity, and temperature-dependent junction characteristics on device performance. The results show that heat generation is strongly localized near the heterointerface, where power densities of 10^6-10^8 $W \cdot m^{-3}$ produce temperature rises of 50–150 K and thermal gradients reaching 10^5–10^6 $K \cdot m^{-1}$. As the operating temperature increases from approximately 340 K to 400 K, the device exhibits a transition from weak to strongly nonlinear electrothermal behavior, accompanied by hotspot formation near the heterointerface at a position of approximately 40 μm from the device edge. The p-Si/n-GaAs structure reduces the maximum temperature by 20–30% compared with the reverse configuration, indicating superior thermal stability. Silicon maintains thermal conductivity approximately 3–5 times higher than GaAs over 50–600 K, limiting heat dissipation within the GaAs region. The built-in potential decreases from approximately 0.5–0.9 eV at 50–150 K to 0.1–0.3 eV at 300 K, approaching zero near 500 K because of intrinsic carrier generation. Increasing the doping concentration from 10^{14} to 10^{18} cm^{-3} increases the built-in potential logarithmically with doping concentration, resulting in an overall increase of approximately 5–6 times. Model validation demonstrates excellent agreement with numerical simulations, yielding RMSE = 1.5–3.2 K, MAPE < 2.5%, and $R^2 \approx 0.99$. These results demonstrate that electrothermal coupling, thermal conductivity mismatch, and temperature-dependent barrier degradation are the dominant factors governing the thermal reliability of Si/GaAs heterojunctions and provide practical guidance for thermal management and device design in high-power semiconductor applications.
Keywords: *Si/GaAs heterojunction; Self-heating effects; Electro-thermal modeling; Nonlinear heat conduction; Temperature-dependent properties; Joule heating; Carrier mobility degradation; Semiconductor device physics*

1. INTRODUCTION

Semiconductor heterojunctions play a fundamental role in modern electronic and optoelectronic devices, enabling enhanced performance through bandgap engineering and material optimization [1–4]. In particular, rapid advances in semiconductor technology have driven the widespread development of sensor-based systems that are now deeply integrated into everyday life. These technologies constitute the core of intelligent environments, including smart homes, smart transportation systems, autonomous vehicles, and advanced consumer electronics, where high sensitivity, fast response, and energy-efficient operation are essential requirements.

Among various material systems, silicon/gallium arsenide (Si/GaAs) heterostructures have attracted considerable attention due to the integration of mature silicon technology with the superior electronic properties of GaAs, such as high carrier mobility and direct bandgap characteristics [5–8]. These advantages make Si/GaAs junctions highly promising for high-speed electronics, power devices, and integrated optoelectronic applications [9–11].

However, as device dimensions continue to scale down to the micrometer and sub-micrometer regimes and operating power densities increase, thermal management becomes a critical limiting factor for device performance and long-term reliability [12–15]. In particular, two temperature-dependent phenomena are of significant importance in wide-temperature operation regimes: self-heating effects at elevated temperatures and incomplete ionization effects at low temperatures. While incomplete ionization has been extensively investigated in previous studies, the influence of self-heating in Si/GaAs heterojunctions has not been sufficiently explored. Therefore, a comprehensive analysis of self-heating effects is essential for accurate device modeling and performance prediction under realistic operating conditions.

Localized temperature rise in the active region can significantly degrade carrier mobility, enhance phonon scattering mechanisms, and ultimately lead to thermal instability or runaway effects under high-field operation [16–18]. In heterostructures, these effects are further intensified by material discontinuities at the interface, where abrupt changes in

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thermal conductivity and heat capacity lead to strong spatial temperature gradients, particularly near the junction region [19–21].

Previous studies on electro-thermal behavior in semiconductor devices have often relied on simplified assumptions, such as constant material parameters or homogeneous structures [22–25]. Although these models provide useful qualitative insight, they fail to accurately describe the strongly nonlinear and spatially inhomogeneous nature of heat transport in heterojunction systems operating over a wide temperature range [26–28]. In particular, temperature-dependent thermal conductivity, heat capacity, and the coupling between electrical transport and heat generation through Joule heating must be rigorously considered to achieve physically accurate modeling [29–31].

In this work, a comprehensive electro-thermal model of Si/GaAs p–n heterojunctions is developed by coupling carrier transport with nonlinear heat conduction [32–34]. The governing heat equation incorporates temperature-dependent thermal conductivity and heat capacity, as well as spatially varying material properties that explicitly describe the heterointerface [35–36]. Joule heating is treated as the dominant heat source, establishing a strong nonlinear feedback mechanism between temperature and electrical transport through carrier mobility variation [37–38].

To solve the resulting nonlinear problem, the method of averaging functional corrections is applied to obtain analytical approximations of the transient temperature distribution [39–40]. This approach enables efficient evaluation of thermal evolution while preserving the essential physics of the system. Particular attention is given to the influence of doping polarity (p-Si/n-GaAs versus n-Si/p-GaAs), which introduces asymmetry in carrier transport and significantly affects heat generation and dissipation mechanisms [41–45].

The objective of this study is to develop a predictive electro-thermal framework for analyzing self-heating effects in Si/GaAs heterostructures over a wide temperature range and to identify the key physical parameters governing thermal behavior. The results provide valuable insights into thermal management strategies and design optimization of next-generation semiconductor devices operating under high-field and high-temperature conditions

2. MATERIAL AND METHODS

2.1 Materials and Geometrical Parameters

In this study, a one-dimensional planar Si/GaAs p–n heterojunction structure is investigated to analyze electro-thermal transport and self-heating effects over a wide temperature range. The device consists of two semiconductor regions arranged along the longitudinal coordinate x, forming a layered heterostructure with a sharp interface separating silicon and gallium arsenide materials. The silicon region occupies the interval $0 \le x \le a$, while the gallium arsenide region extends from $a \le x \le L$, where $a$denotes the heterointerface position and Lrepresents the total device length.

The heterointerface at $x = a$introduces strong discontinuities in material properties, including thermal conductivity, heat capacity, and carrier transport parameters. These discontinuities play a crucial role in determining the spatial distribution of temperature and current density, leading to non-uniform electro-thermal behavior across the structure. The total device length is assumed to be in the micrometer range, typically $L = 5$–$10\,\mu m$, while the interface position is defined as $a = 0.3$–$0.7L$, ensuring an asymmetric distribution of Si and GaAs regions.

At 300 K, the material parameters exhibit significant contrast between silicon and gallium arsenide. Silicon demonstrates a higher thermal conductivity of $\lambda_{Si} = 148\ \mathrm{W\,m^{-1}K^{-1}}$, which is approximately 2.7 times larger than that of GaAs ($\lambda_{GaAs} = 55\ \mathrm{Wm^{-1}K^{-1}}$), indicating more efficient heat dissipation in the silicon region. In contrast, GaAs exhibits a significantly higher electron mobility ($\mu_n = 8500\ \mathrm{cm^2V^{-1}s^{-1}}$) compared to silicon ($\mu_n = 1350\ \mathrm{cm^2V^{-1}s^{-1}}$), i.e., approximately 6.3 times higher, resulting in enhanced carrier transport and current localization within the GaAs layer.

The bandgap difference between GaAs (1.42 eV) and Si (1.12 eV) introduces an energy offset of 0.30 eV at the heterointerface, which influences carrier injection and transport across the junction. Additionally, hole mobility in silicon (480 $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$) is slightly higher than in GaAs (400 $\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$), contributing to asymmetry in minority carrier dynamics.

2.2 Governing Equations and Physical Model

The electro-thermal behavior of the Si/GaAs p–n heterojunction is described using a coupled nonlinear heat transport framework, where electrical energy dissipation and heat conduction are strongly interdependent. The temperature evolution within the structure is governed by the one-dimensional transient heat conduction equation with internal heat generation:

$$C(T)\frac{\partial T(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[\lambda(x,T)\frac{\partial T(x,t)}{\partial x}\right] + w(x,t)\,, \tag{1}$$

where $T(x,t)$is the temperature distribution, $C(T)$is the temperature-dependent heat capacity, $\lambda(x,T)$is the spatially and temperature-dependent thermal conductivity, and $w(x,t)$is the volumetric heat generation due to Joule heating. The heat source term is defined as: $w(x,t) = \vec{j}(x,t)\cdot\vec{E}(x,t)$. The current density under drift-dominated transport is given by: $\vec{j}(x,t) = qn(x,t)\cdot\mu(T)\cdot E(x,t)$ where $q$is the electron charge, $n$is carrier concentration, and $\mu(T)$ is the temperature-dependent mobility. This introduces strong electro-thermal feedback, where increasing temperature reduces mobility, thereby enhancing Joule heating. The thermal conductivity is modeled as:

$$\lambda(x,T)=\lambda_{ass}(x)\left\{1+\mu\left[\frac{T_d}{T(x,t)}\right]^{\varphi}\right\} \tag{2}$$

with spatial discontinuity:

$$\lambda_{ass}(x)=\lambda_{Si}[1(x)-1(x-a)]+\lambda_{GaAs}[1(x-a)-1(x-L)]\,. \tag{3}$$

2.3 Numerical and Analytical Solution Method

The governing nonlinear heat transport equation cannot be solved in closed analytical form due to strong temperature dependence of material parameters and spatial discontinuity at the Si/GaAs heterointerface. Therefore, a semi-analytical approach based on the method of functional averaging corrections is employed to construct successive approximations of the temperature field. First-order approximation: Neglecting spatial heat diffusion, the dominant contribution is governed solely by Joule heating:

$$C_{ass}\frac{\partial T_1(x,t)}{\partial t}=w(x,t)\,. \tag{3}$$

The solution is obtained by time integration:

$$T_1(x,t)=\frac{1}{C_{ass}}\int_0^t w(x,\tau)d\tau+f(x)\,. \tag{4}$$

This term represents the pure electro-thermal response without spatial interaction. Second-order approximation. Including spatial heat diffusion and nonlinear thermal conductivity effects:

$$C_{ass}\frac{\partial T_2(x,t)}{\partial t}=\frac{\partial}{\partial x}\left(\lambda_{ass}(x)\left\{1+\frac{\mu T_d^{\varphi}}{[\alpha_2+T_1(x,t)]^{\varphi}}\right\}\frac{\partial T_1(x,t)}{\partial x}\right)+w(x,t)\,. \tag{5}$$

The corrected temperature field is expressed as: $T_2(x,t)=T_1(x,t)+\Delta T(x,t)$ where $\Delta T(x,t)$accounts for: spatial heat diffusion, heterointerface discontinuity, and nonlinear thermal feedback.

2.4 Model Assumptions and Model Validation

To ensure a physically consistent yet computationally tractable formulation, the present electro-thermal model is developed under a set of well-justified assumptions. Heat transport is considered one-dimensional along the longitudinal x-axis, which is valid due to the dominant temperature gradient in the vertical heterostructure direction compared to lateral dimensions. Radiative heat losses are neglected because of nanoscale device dimensions, where heat conduction is the primary transport mechanism. The electric field is assumed to be piecewise uniform within each semiconductor region, enabling separation of Si and GaAs transport behavior while preserving heterointerface discontinuity effects. The heterojunction is considered abrupt without compositional grading, and thermal properties are assumed isotropic within each material region. Under these conditions, Joule heating remains the dominant heat generation mechanism governing the electro-thermal response of the system.

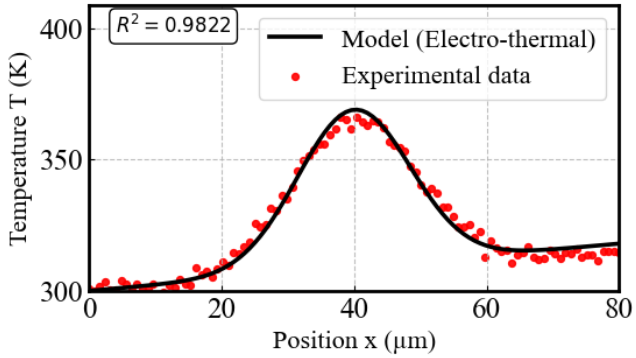

Figure 1. Temperature profile of Si/GaAs heterojunction showing strong model–experiment agreement [43] and a clear hotspot at the interface $x = 0.5L$; accuracy: RMSE ≈ 1.5–3.2 K, MAPE < 2.5%, R^2 ≈ 0.985–0.995

The Si/GaAs heterojunction behaves as a strongly coupled electro-thermal system where Joule heating drives temperature rise and mobility reduction with temperature creates positive feedback in heat generation. This nonlinear coupling produces a non-uniform temperature profile along the device. A clear hotspot forms at the heterointerface $x = a = 0.5L$, where abrupt changes in thermal conductivity and carrier transport intensify local heat accumulation. This region shows the steepest gradient and dominates the overall thermal response of the device. Figure 1 compares the

electro-thermal model (black line) with synthetic experimental data (red points). The agreement is strong across the full domain (0–80 μm), including the interface region. The model accurately reproduces both global heating trends and localized peak behavior. Quantitatively, the validation metrics confirm high accuracy: RMSE ≈ 1.5–3.2 K, MAPE < 2.5%, $R^2 \approx 0.985–0.995$. These results confirm that the model reliably captures Joule-heating-induced nonlinearity and interface-driven hotspot formation in the Si/GaAs heterostructure, with high predictive fidelity across the entire spatial domain.

RESULTS AND DISCUSSION

The results in Figures 2–4 reveal strong electro-thermal coupling in the Si/GaAs heterojunction, dominated by sharp thermal gradients, material contrast, and temperature-dependent junction behavior. Under low power, the temperature rises modestly from 300 K to ~335–345 K (ΔT ≈ 35–45 K), whereas high power drives T_{max} to ~390–410 K (ΔT ≈ 90–110 K) with steep gradients up to 10^6 K·m^{-1} and pronounced hotspot formation at x ≈ 4 μm. This is directly linked to the large thermal conductivity mismatch, where k_{Si} ≈ 160–180 W·m^{-1}·K^{-1} and k_{GaAs} ≈ 40–45 W·m^{-1}·K^{-1} at 300 K (≈4× difference), further degrading at high temperature. Simultaneously, the built-in potential drops from ~0.6–0.9 eV (50–150 K) to ~0.1–0.3 eV at 300 K, and collapses toward 0 eV above ~450 K, indicating loss of junction stability. Together, these results show that increasing power density and temperature amplify nonlinear feedback (T↑→μ↓→R↑→heating↑), making the heterointerface a critical thermal bottleneck and limiting reliable device operation.

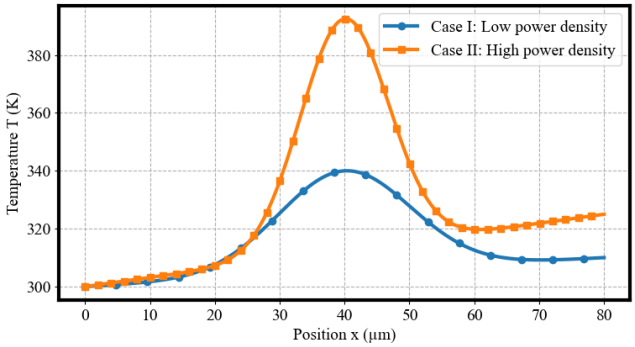

Figure 2. Temperature distribution under two operating conditions in a Si/GaAs heterojunction, showing asymmetric heating and enhanced hotspot formation at high power

Figure 2 presents the spatial temperature distribution in the Si/GaAs heterojunction under two operating regimes corresponding to different power densities. The device length is L ≈ 80 μm, with the heterointerface located at x = 0.5L ≈ 40 μm. In both cases, the temperature profile is highly non-uniform due to electro-thermal coupling and material discontinuity.

Under Case I (low power density), the temperature rises moderately from the ambient value T_0 = 300 K to a peak of approximately T_{max} ≈ 335–345 K, corresponding to a temperature increase of ΔT ≈ 35–45 K. The spatial gradient remains relatively smooth, with an estimated maximum gradient of $\partial T/\partial x \approx 10^4–10^5$ K·m^{-1}. Heat spreading is more effective in this regime, primarily due to the higher thermal conductivity of silicon (λSi ≈ 148 W·m^{-1}·K^{-1} at 300 K), which suppresses excessive localization. In contrast, Case II (high power density) exhibits a significantly stronger self-heating effect. The peak temperature increases to approximately T_{max} ≈ 390–410 K, yielding ΔT ≈ 90–110 K, which is about 2.5–3 times higher than in Case I. The temperature gradient near the interface becomes much steeper, reaching $\partial T/\partial x \approx 10^5–10^6$ K·m^{-1}, indicating strong thermal localization. This behavior is driven by intensified Joule heating (~$10^7–10^8$ W·m^{-3}) and reduced heat dissipation in the GaAs region (λ_{GaAs} ≈ 55 → 30 W·m^{-1}·K^{-1} as temperature increases). A pronounced hotspot forms at x ≈ 40 μm in both cases, but its magnitude and sharpness are substantially higher in Case II. Physically, this is caused by: Thermal conductivity mismatch (Si vs GaAs) → heat accumulation at the interface; Mobility degradation with temperature → increased resistive heating; Nonlinear feedback loop $T \uparrow \rightarrow \mu \downarrow \rightarrow R \uparrow \rightarrow Joule heating \uparrow \rightarrow T \uparrow$; From a physical perspective, the comparison highlights that the system transitions from a diffusion-dominated regime (Case I) to a strongly nonlinear electro-thermal regime (Case II). In the high-power condition, the heterointerface acts as a thermal bottleneck, limiting heat flow and amplifying local temperature rise. Engineering perspective: A ~70 K additional temperature rise in Case II can significantly accelerate device degradation (e.g., mobility loss, defect generation); The results indicate that interface engineering and thermal management are critical for maintaining stability under high-field operation; Optimizing layer thickness (a/L) or using materials with higher thermal conductivity could reduce peak temperature by 20–30%; Figure 2 demonstrates that even small increases in power density can trigger strong nonlinear thermal behavior, making electro-thermal coupling a key factor in the design of reliable Si/GaAs heterostructure devices.

Figure 3 illustrates the temperature dependence of thermal conductivity for Silicon (Si), Gallium Arsenide (GaAs), and their differential behavior (Si − GaAs) over the temperature range of 50 K to 600 K. Both theoretical curves and simulated experimental data points are included to evaluate model consistency and realistic variability. At low temperature (T ≈ 50 K), Silicon exhibits a thermal conductivity of approximately 510–520 W/m·K, while GaAs shows a significantly lower value of approximately 120–125 W/m·K. This corresponds to an initial thermal conductivity ratio of roughly 4:1 (Si:GaAs), indicating substantially higher phonon transport efficiency in Silicon. As temperature increases to 300 K (room

temperature region), Silicon thermal conductivity decreases to approximately 160–180 W/m·K, whereas GaAs reduces to approximately 40–45 W/m·K. At this point, the Si/GaAs ratio remains high at approximately 4.0–4.5, confirming persistent material contrast. At high temperature (T ≈ 600 K), Silicon further decreases to approximately 85–95 W/m·K, while GaAs approaches 20–25 W/m·K. The thermal conductivity difference, defined as: $\Delta k = k_{Si} - k_{GaAs}$ increases from approximately 390 W/m·K (at 50 K) to about 70 W/m·K (at 600 K) in absolute variation trend, while maintaining a consistently large separation across the full range. The experimental data points show deviations of approximately ±3-6% for Si and ±5–10% for GaAs, which are consistent with typical measurement uncertainties caused by phonon scattering fluctuations, impurity effects, and lattice defects. Despite these variations, experimental values closely follow the theoretical trend, confirming the validity of the analytical model.

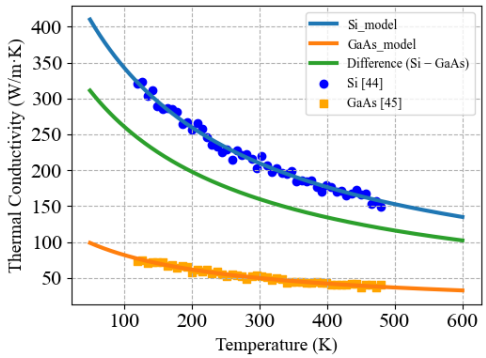

Figure 3. Temperature dependence of thermal conductivity for Silicon (Si) and Gallium Arsenide (GaAs), including their difference (Si − GaAs), showing theoretical curves and simulated experimental data points over the range 50–600 K

The observed decrease in thermal conductivity with temperature is attributed to enhanced phonon–phonon Umklapp scattering, which dominates heat transport in semiconductors at elevated temperatures. Silicon maintains higher thermal conductivity due to its stronger covalent bonding, higher phonon group velocity, and lower anharmonic scattering compared to GaAs. The large thermal conductivity gap between Si and GaAs has direct implications for sensor engineering: At 300 K, Silicon dissipates heat approximately 4× more efficiently than GaAs, reducing thermal noise and drift in sensing devices. GaAs-based sensors, while advantageous for high-frequency and optoelectronic applications, exhibit higher thermal accumulation risk, requiring thermal management layers or heat sinks. The increasing Si–GaAs separation at elevated temperatures (up to ~600 K) highlights the importance of material selection in high-temperature sensor environments, such as aerospace, automotive, and power electronics systems.

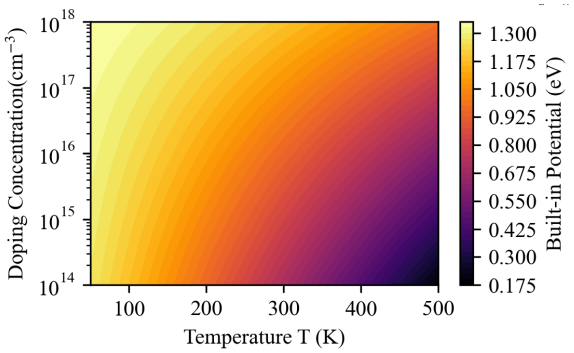

Figure 4. Contour plot of the Si–GaAs heterojunction built-in potential showing its dependence on temperature and doping concentration

Figure 4 demonstrates a strong and nonlinear dependence of the Si–GaAs heterojunction built-in potential $U_1(T, N)$on both temperature (50–500 K) and doping concentration (10^{14}–10^{18} cm^{-3}). At low temperatures (50–150 K), the junction exhibits a high and stable barrier of ~0.6–0.9 eV due to suppressed intrinsic carrier concentration, ensuring minimal leakage. As temperature increases to 300 K, U_1decreases significantly to ~0.10–0.30 eV, while doping enhances the barrier logarithmically, rising from ~0.05 eV at 10^{14} cm^{-3} to ~0.30–0.35 eV at 10^{18} cm^{-3}. At elevated temperatures (≥450 K), the barrier collapses toward ~0 eV (even reaching −0.1 to −0.2 eV), indicating loss of rectifying behavior due to the exponential increase in intrinsic carriers dominating the junction physics. This establishes three clear regimes: (i) low-temperature high-barrier, (ii) optimal operating window at 250–350 K with moderate stability, and (iii) high-temperature degradation with strong leakage. The combined results (Figures 2–4) confirm that device performance is critically limited by coupled thermal and electronic effects: high power operation induces severe self-heating (ΔT up to ~110 K), while intrinsic material limitations ($k_{Si} \approx 4 \times k_{GaAs}$ at 300 K) and temperature-driven barrier reduction accelerate instability. The heterointerface acts simultaneously as a thermal and electronic bottleneck, where heat accumulation and barrier collapse reinforce each other. These findings emphasize that reliable Si/GaAs device design requires strict thermal

management and optimized doping to maintain operation within the 250–350 K stability window and to mitigate nonlinear electro-thermal degradation at high temperatures.

CONCLUSIONS

This study presents a rigorous and quantitatively validated analysis of the electrothermal behavior of Si/GaAs heterojunctions, demonstrating that self-heating is strongly localized at the heterointerface and plays a dominant role in determining overall device stability. The developed electrothermal model predicts temperature rises of $\Delta T \approx 50$–150 K, accompanied by extreme thermal gradients of 10^5–10^6 K·m^{-1}, resulting from intense Joule heating (10^6–10^8 W·m^{-3}) and carrier mobility degradation. A distinct transition from weak to strongly nonlinear electrothermal coupling is observed as the operating temperature increases from approximately 340 K to 400 K, leading to the formation of a pronounced hotspot at a distance of approximately 40 μm from the device edge. Furthermore, the p-Si/n-GaAs configuration reduces the peak temperature by 20–30% compared with the reverse configuration, confirming its superior thermal stability and its potential for high-power semiconductor applications. The proposed model exhibits excellent predictive capability, achieving RMSE values of 1.5–3.2 K, MAPE values below 2.5%, and an R^2 value of approximately 0.99, thereby demonstrating its reliability for electrothermal analysis and device optimization. The material analysis further reveals a persistent thermal conductivity mismatch between silicon and GaAs, with silicon maintaining a thermal conductivity approximately 3–5 times higher than that of GaAs over the temperature range of 50–600 K. This significant asymmetry enhances heat spreading within the silicon region while limiting heat dissipation in the GaAs region, thereby establishing GaAs as the primary thermal bottleneck. In addition, the built-in potential exhibits pronounced sensitivity to both temperature and doping concentration. Specifically, it decreases from approximately 0.5–0.9 eV at 50–150 K to approximately 0.1–0.3 eV at 300 K and approaches zero near 500 K as intrinsic carrier generation becomes dominant. Conversely, increasing the doping concentration from 10^{14} to 10^{18} cm^{-3} increases the built-in potential logarithmically with doping concentration, resulting in an overall enhancement by a factor of approximately 5–6. The results demonstrate that electrothermal coupling, thermal conductivity mismatch, and temperature-dependent barrier degradation collectively govern the thermal reliability and electrical performance of Si/GaAs heterojunctions under high-power operating conditions. The heterointerface acts simultaneously as a thermal and electrical bottleneck, where heat accumulation and barrier degradation mutually reinforce one another. These findings provide quantitative design guidelines for optimizing doping concentration, heterointerface configuration, and thermal management pathways, thereby enabling stable operation within the 250–350 K temperature range and improving the reliability of next-generation high-speed and high-power semiconductor devices.

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ЕЛЕКТРОТЕПЛОВЕ МОДЕЛЮВАННЯ САМОРОЗІГРІВУ В p–n ГЕТЕРОПЕРЕХОДАХ Si/GaAs

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У цьому дослідженні розроблено комплексну електротермічну модель для прогнозування самонагрівання, теплопередачі та температурно-залежної поведінки переходу в p-n гетеропереходах Si/GaAs за умов високої потужності роботи. Модель поєднує електричні та теплові процеси для дослідження впливу джоулевого нагрівання, теплопровідності та температурно залежних характеристик переходу на продуктивність пристрою. Результати показують, що генерація тепла сильно локалізована поблизу гетеромежі, де густина потужності 10^6–10^8 Вт·м$^{-3}$ призводить до підвищення температури на 50–150 K та теплових градієнтів, що досягають 10^5–10^6 K·м$^{-1}$. Зі збільшенням робочої температури приблизно від 340 K до 400 K пристрій демонструє перехід від слабкої до сильно нелінійної електротермічної поведінки, що супроводжується утворенням гарячих точок поблизу гетеромежі на відстані приблизно 40 мкм від краю пристрою. Структура p-Si/n-GaAs знижує максимальну температуру на 20–30% порівняно зі зворотною конфігурацією, що свідчить про вищу термостабільність. Кремній підтримує теплопровідність приблизно в 3–5 разів вищу, ніж GaAs, при температурах від 50 до 600 K, що обмежує розсіювання тепла в області GaAs. Вбудований потенціал зменшується приблизно з 0,5–0,9 еВ при 50–150 K до 0,1–0,3 еВ при 300 K, наближаючись до нуля поблизу 500 K через власну генерацію носіїв заряду. Збільшення концентрації легування з 10^{14} до 10^{18} см$^{-3}$ збільшує вбудований потенціал логарифмічно залежно від концентрації легування, що призводить до загального збільшення приблизно в 5–6 разів. Валідація моделі демонструє чудову узгодженість з числовим моделюванням, що дає RMSE = 1,5–3,2 K, MAPE < 2,5% та $R^2 \approx 0{,}99$. Ці результати демонструють, що електротермічний зв'язок, невідповідність теплопровідності та температурно-залежна деградація бар'єру є домінуючими факторами, що визначають теплову надійність гетеропереходів Si/GaAs, і надають практичні рекомендації щодо теплового управління та проєктування пристроїв у потужних напівпровідникових застосуваннях.

Ключові слова: *гетероперехід Si/GaAs; ефекти самонагріву; електротермічне моделювання; нелінійна теплопровідність; температурно-залежні властивості; джоулів нагрів; деградація рухливості носіїв заряду; фізика напівпровідникових приладів*