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TCAD-BASED CAPACITANCE ANALYSIS FOR IDENTIFYING LONGITUDINALLY LOCALIZED OXIDE-TRAPPED CHARGE IN SOI FinFETS

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This study examines the effect of the spatial position of locally trapped oxide charge on the gate-to-source and gate-to-drain capacitances of an SOI FinFET using three-dimensional TCAD Sentaurus simulations. The results reveal that the location of the trapped charge strongly influences the gate-to-source capacitance via charge-carrier redistribution near the channel surface, whereas a distinct response is observed when the trapped charge is near the oxide edge. Moreover, the gate-drain-to-gate-source capacitance ratio varies systematically with the trapped-charge position along the channel, suggesting that this parameter can serve as a reliable electrical indicator for detecting oxide-trapped charge and estimating its spatial distribution in FinFET devices.
Keywords: *SOI FinFET; Oxide trapped charge; Gate-source capacitance; Gate-drain capacitance; Charge distribution; TCAD simulation*

INTRODUCTION

Metal–oxide–semiconductor field-effect transistors (MOSFETs), particularly Fin field-effect transistors (FinFETs), are highly susceptible to various electrical stresses and radiation-induced effects during operation, which may degrade their electrical characteristics. Among the most significant degradation mechanisms are hot-carrier injection [1-3], bias temperature instability [4], off-state stress, and radiation-induced charge buildup [5]. These effects arise primarily from charge injection into, or generation within, the oxide layer and at the semiconductor–oxide interface. Since such degradation directly influences the performance and reliability of analog and digital integrated circuits, its impact must be carefully considered in modern device design. Oxide-trapped charge can alter key MOSFET parameters, including the threshold voltage, subthreshold swing, and transconductance, thereby deteriorating the overall device performance. For this reason, the development of reliable methods for identifying the localization and spatial distribution of trapped charge along the channel is of considerable importance. One of the simplest and fastest diagnostic approaches for detecting charge trapped in the oxide or at the interface is based on capacitance–voltage measurements of lateral source(dr.)-channel p–n junctions [6-9]. Previous studies have shown that a nonuniform charge distribution in the oxide layer or at the semiconductor–oxide interface is reflected in the electrical behavior of source–channel and drain–channel p–n junctions. Therefore, the longitudinal distribution of trapped charge along the channel should also affect other capacitances associated with these lateral junctions [10–12]. In the present work, this approach, originally proposed for planar MOSFETs, is adapted for application to SOI FinFET structures. The underlying concept is based on the sensitivity of lateral source–channel and drain–channel p–n junction capacitances to oxide- and interface-trapped charge [13–14]. Accordingly, the most suitable electrical configuration for such an analysis is one in which the capacitance of the lateral source–channel (drain–channel) p–n junction, $C_{p\text{-}n}$ makes a substantial contribution to the measured total capacitance. In SOI FinFETs, one of the relevant configurations satisfying this condition is the gate–source (or gate–drain) connection, as illustrated in Fig. 1.

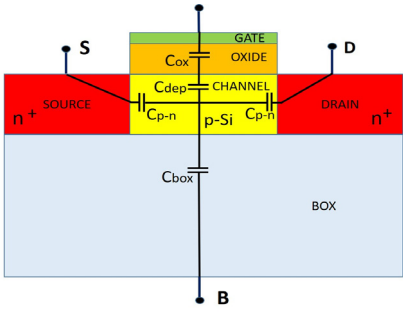

Figure 1. Cross-section of the simulated SOI FinFET with capacitances between contacts

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The gate–source and gate–drain configurations in the considered SOI FinFET can be represented by a series combination of three capacitance components: the gate-oxide capacitance C_{ox}, the depletion-layer capacitance at the oxide–semiconductor interface C_{dep}, and the source–channel p–n junction capacitance C_{p-n}. Among these contributions, C_{dep} becomes significant only when the device operates in the depletion regime. In the present analysis, however, only the barrier capacitance of the source–channel p–n junction is considered. To satisfy this condition, a positive voltage is applied to the n-type source with respect to the gate, thereby establishing carrier accumulation near the oxide-semiconductor interface. Under such bias conditions, the contribution of the depletion-layer capacitance can be neglected, and the total gate–source capacitance is determined predominantly by the series coupling between C_{ox} and C_{p-n}. Accordingly, the resulting capacitance can be written as

$$C_{gs} = \frac{C_{p-n} \cdot C_{ox}}{C_{p-n} + C_{ox}} \tag{1}$$

where C_{ox} denotes the gate-oxide capacitance per unit area and is essentially independent of the applied voltage.

Since the estimated depletion width of the source–channel (or drain–channel) p–n junction is about 0.1 μm, whereas the gate-oxide thickness is only t_{ox}=2.5 nm, the junction capacitance C_{p-n} remains much smaller than C_{ox}. As a consequence, the equivalent capacitance C_{gs} is governed mainly by C_{p-n}, making it highly sensitive to electrostatic perturbations associated with oxide-trapped charge. This feature is particularly important for charge-diagnostics applications, because any local trapped charge in the oxide modifies the potential distribution in the channel region and, in turn, alters the depletion characteristics of the lateral p–n junction. Therefore, variations in C_{gs} can be directly related to the spatial localization of trapped charge along the channel. On this basis, the present work focuses on simulating the dependence of C_{gs} on the position of a local oxide-trapped charge in the SOI FinFET structure.

MATERIALS AND METHODS

Three-dimensional numerical simulations were performed using the Advanced TCAD Sentaurus platform to investigate the effect of localized oxide-trapped charge on the capacitance characteristics of an SOI FinFET structure. The capacitance–voltage (C-V) response of the gate–source and gate–drain configurations was analyzed using a small-signal AC simulation at 1 MHz. This method was selected because it provides a reliable means of evaluating capacitance variations caused by local electrostatic perturbations in nanoscale transistor structures.

The geometry of the simulated SOI FinFET is illustrated in Fig. 2. The gate length, L_{gate}, was fixed at 25 nm, while the gate oxide thickness was taken as 2.5 nm. The silicon channel thickness, T_{Si}, and buried oxide thickness, T_{box}, were set to 30 nm and 100 nm, respectively. The channel width was chosen as 12 nm. The active channel region was assumed to be p-type silicon with a doping concentration of 1×10^{15} cm^{-3}. These geometrical and doping parameters were selected to represent a realistic SOI FinFET structure suitable for analyzing the sensitivity of gate-related capacitances to trapped-charge effects.

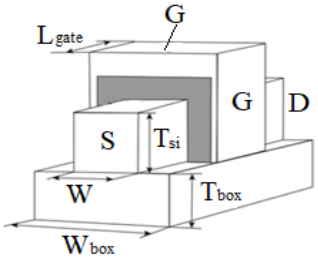

Figure 2. 3D structure of the simulated SOI FinFET

The gate–source capacitance, C_{gs}, was simulated for different positions of a localized trapped charge in the oxide layer, with the position defined by the distance between the center of the charged region and the source–channel boundary. It should be noted that L does not represent the depth of the trapped charge across the oxide thickness. In all simulations, the localized charged region remains embedded inside the gate oxide, while only its longitudinal position along the channel direction is varied. Thus, L is measured from the source–channel boundary to the center of the charged region along the source-to-drain direction. The case L=2.5 nm corresponds to the position where the 5 nm-long charged region touches the source-side edge of the gate oxide, and it does not imply that the charge is located inside the semiconductor. The local oxide-trapped charge was modeled as a uniformly charged region embedded in the oxide. The charge density in this region was set to 10^{12} cm^{-2} (equivalent to 4×10^{18} cm^{-3}), which is a physically reasonable value for trapped charge that may occur in MOSFET structures under electrical or radiation-induced stress conditions. The characteristic size of the local charged region along the channel direction was fixed at d = 5 nm.

Since the depletion width of the lateral source–channel (drain–channel) p–n junction exceeds the channel length, a local trapped charge situated at a distance L from the source–channel junction can appreciably modify the carrier distribution inside the channel [15,16]. This electrostatic perturbation is expected to affect the junction capacitance and, consequently, the overall C–V behavior of the gate–source connection. Owing to the structural symmetry of the FinFET with respect to the channel center, the gate–source and gate–drain capacitances are expected to exhibit equivalent behavior

under symmetric conditions. For this reason, the present analysis is focused primarily on the gate–source capacitance, while the behavior of the gate–drain capacitance can be inferred from the device symmetry.

RESULTS AND DISCUSSION

The simulated C–V characteristics of the gate–source capacitance, C_{gs}, are presented in Fig. 3. In Fig. 3, each curve corresponds to a different longitudinal position L of the localized oxide-trapped charge. Here, L denotes the distance from the source–channel boundary to the center of the localized charged region along the channel direction. The reference curve corresponds to the case without trapped charge, while the other curves represent different values of L, as indicated in the legend. As can be observed, the capacitance behavior is strongly influenced by the position of the local oxide-trapped charge along the channel. At relatively high applied voltages, C_{gs} exhibits a pronounced and nearly monotonic dependence on the trapped-charge location, indicating that the electrostatic effect of the localized charge becomes increasingly important under these bias conditions. This trend is more clearly illustrated in Fig. 4, where the capacitance is plotted as a function of the distance L. An exceptional behavior is observed for the case L = 2.5 nm (point B in Fig. 4). This deviation from the general monotonic trend can be attributed to the fact that, at this position, the local charged region comes into direct contact with the edge of the oxide layer. Such a configuration modifies the local electrostatic environment differently from the other trapped-charge positions and leads to a distinct capacitance response. Therefore, although the overall trend confirms a systematic dependence of C_{gs} on the trapped-charge position, the oxide-edge case should be considered separately due to its specific geometrical and electrostatic conditions.

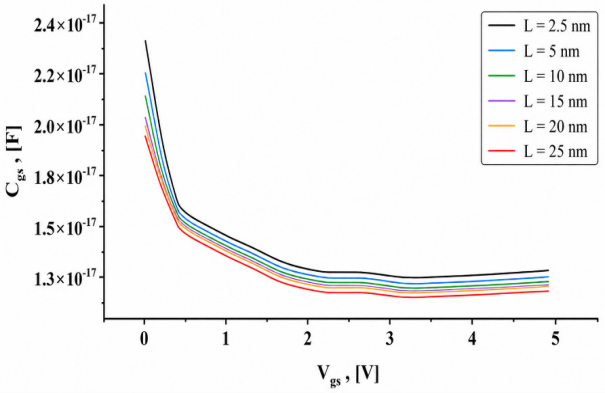

Figure 3. C–V characteristics of the gate–source capacitance, C_{gs}, for different longitudinal positions L of the localized oxide-trapped charge in the gate oxide. The reference curve corresponds to the case without a trapped charge. The legend indicates the corresponding L value for each curve

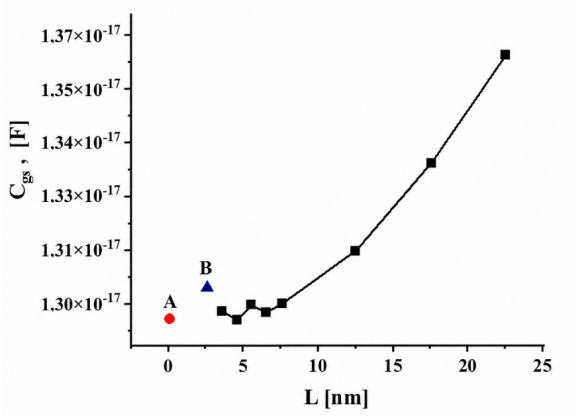

Figure 4. Figure 4. Dependence of C_{gs} on the longitudinal position L of the localized oxide-trapped charge at V_{gs}=4.5 V. Point A corresponds to the reference case without trapped charge, whereas point B corresponds to L=2.5 nm, where the localized charged region touches the source-side edge of the gate oxide

The increase in C_{gs} is attributed to the influence of locally trapped charge in the oxide on the channel carrier concentration. To avoid ambiguity in charge localization, Fig. 5 includes a schematic inset showing the gate oxide, the silicon channel, the source–channel boundary, and the longitudinal positions of the localized trapped charge under investigation. The grey region represents the localized charged domain embedded inside the gate oxide. During the simulation, this charged region is shifted only along the channel direction, whereas its position across the oxide thickness is kept fixed. As shown in Fig. 5, the presence of trapped charge in the oxide layer increases the electron concentration near the channel surface, thereby increasing the gate–source capacitance. From a physical perspective, this behavior reflects the sensitivity of capacitance to charge redistribution in the near-surface region of the channel. By definition, the capacitance can be expressed as follows:

$$C_{gs} = dQ_V/dV. \quad (2)$$

Here, dQ_V represents the change in charge stored in the Cgs capacitance in response to a change in applied voltage, dV.

When a local charge is trapped in the gate oxide, the electron concentration in the channel is modified, which gives rise to an additional charge variation, denoted as dQ_{LC}, in the gate–source capacitance. Consequently, Eq. (2) can be reformulated as follows:

$$C_{gs} = (dQ_V + dQ_{LC})/ dV. \quad (3)$$

This expression explains the increase observed in the gate–source capacitance, C_{gs}, as a consequence of the additional charge redistribution induced by the localized oxide-trapped charge. In the simulated SOI FinFET structure, the maximum variation of C_{gs} caused by the localized trapped charge is approximately 5%. Although this magnitude of variation may appear moderate and does not necessarily indicate severe degradation of the transistor's static current–voltage characteristics, it remains physically meaningful and important for capacitance-based defect diagnostics. The

significance of this variation lies in its systematic dependence on the longitudinal position of the trapped charge. In other words, the change in C_{gs} is not random but follows a clear trend as the localized charge is shifted along the channel. Such a position-dependent capacitance response indicates that the gate–source capacitance is sensitive to local electrostatic perturbations caused by oxide-trapped charge. Therefore, even a several-percent change in capacitance can serve as an electrical signature for detecting localized trapped charge and estimating its approximate position along the channel.

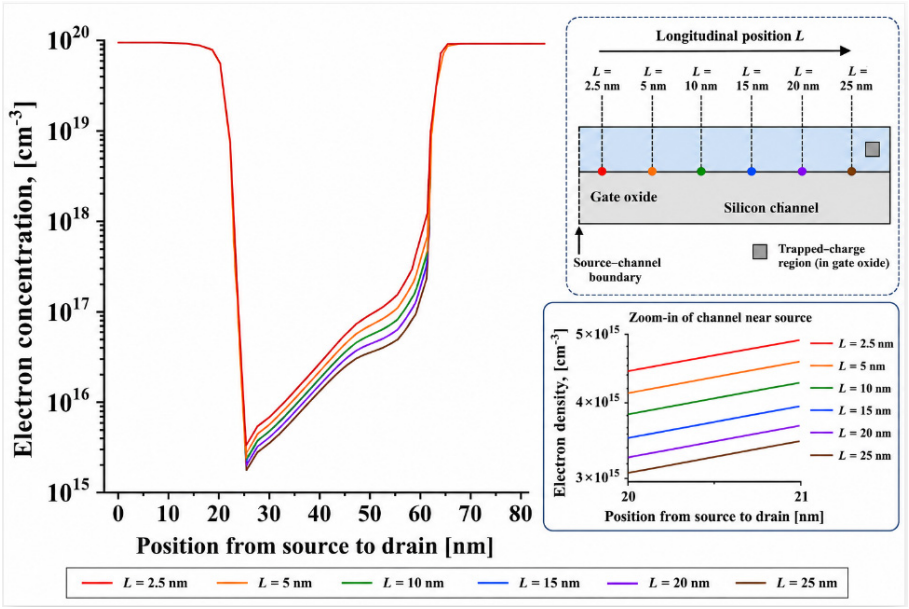

Figure 5. Electron density distribution along the channel at a depth of 2 nm from the channel surface for different longitudinal positions L of the localized oxide-trapped charge. The inset schematically shows the investigated charge positions inside the gate oxide; the charged region remains embedded in the oxide and is shifted only along the source-to-drain direction.

From a device-operation perspective, gate-related capacitances in nanoscale FinFETs contribute to parasitic capacitance, small-signal response, signal delay, and switching behavior. Therefore, a 5% variation in C_{gs} may become relevant in highly scaled devices and in circuits where capacitance matching, transient response, or high-frequency performance is important. However, in the context of the present work, the observed variation should primarily be interpreted not as evidence of catastrophic transistor degradation, but as a measurable and reproducible diagnostic indicator of localized oxide-trapped charge. Thus, the results demonstrate that capacitance variations of this magnitude can be useful for reliability monitoring and defect localization analysis in SOI FinFET structures.

At position L= 2.5 nm of the oxide trapped charge the configuration of the capacitance C_{gs} is changed because the local charge will be in contact with the end of the oxide layer (Fig. 6). In this case the electron density in the channel surface will be redistributed which result in sufficiently increasing the capacitance C_{gs} more than in unbiased case and relatively capacitances corresponding to other positions (Fig. 3). At high applied voltages the redistribution of the carrier densities leads to increasing the C_{gs} with increasing L (Fig. 7).

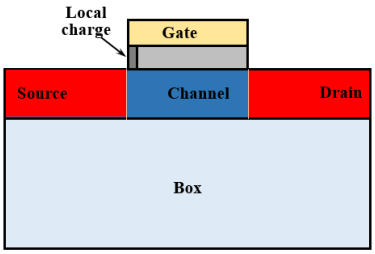

Figure 6. Cross-section of the FinFET with a local charge trapped in the oxide, which is located at the end of the oxide layer. L=2.5 nm.

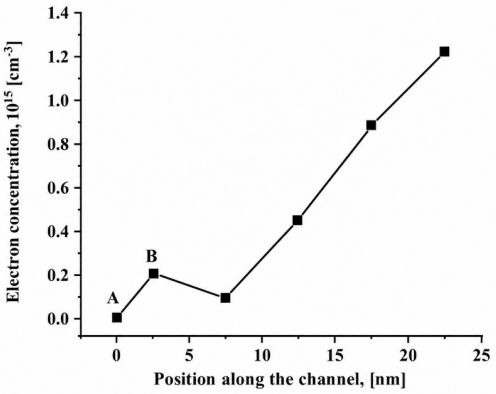

Figure 7. The change in electron density in the channel at a depth of 2 nm from the surface traps local charge in the oxide layer at different positions. A is point is the case without trapped charge, and B is the position with L=2.5 nm

Owing to the structural symmetry of the FinFET, the dependence of the gate–drain capacitance, C_{gd}, on the trapped-charge position L is expected to exhibit a trend opposite to that of the gate–source capacitance, C_{gs}. In other words, as L

increases, C_{gd} decreases, as illustrated in Fig. 8. The positional dependences of both C_{gs} and C_{gd} can therefore be utilized to estimate the location of the oxide-trapped charge along the channel. In this context, the ratio C_{gs}/C_{gd} provides a particularly convenient diagnostic parameter, as shown in Fig. 9. It can be seen that when the trapped charge is located on the source side of the channel center, the ratio C_{gs}/C_{gd} is less than unity, whereas it becomes greater than unity when the trapped charge is positioned on the drain side. If the trapped charge is located at the channel center, the ratio C_{gs}/C_{gd} approaches unity.

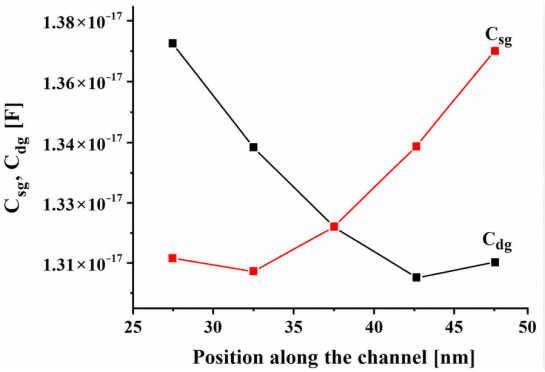

Figure 8. C_{gs} and C_{gd} dependence on the position of the local oxide trapped charge along the channel

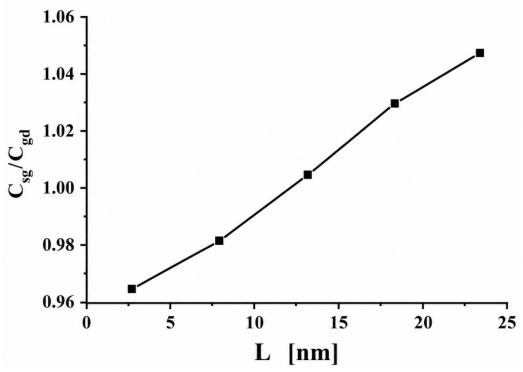

Figure 9. The ratio C_{gs}/C_{gd} dependence on the position of the local oxide trapped charge along the channel

CONCLUSIONS

In this work, the influence of a local oxide-trapped charge on the gate-source and gate-drain capacitances of an SOI FinFET was systematically analyzed using 3D TCAD simulations with the small-signal AC method. The results show that the gate-source capacitance increases monotonically as the trapped charge shifts from the source-side region toward the channel center, except when the charge is positioned at the oxide edge. This behavior is governed by the redistribution of electron concentration near the channel surface induced by the trapped charge. Owing to the device's structural symmetry, the gate-drain capacitance shows the opposite trend, while the Cgs/Cgd ratio varies regularly with the trapped-charge position along the channel. These findings confirm that even a moderate, approximately several-percent variation in gate-related capacitance can serve as a useful diagnostic indicator for identifying localized oxide-trapped charge and estimating its longitudinal position in SOI FinFET structures.

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АНАЛІЗ ЄМНОСТІ НА ОСНОВІ TCAD ДЛЯ ІДЕНТИФІКАЦІЇ ПОЗДОВЖНЬОГО ЛОКАЛІЗОВАНОГО ЗАРЯДУ, ЗАХОПЛЕНОГО ОКСИДОМ, У SOI FinFETS

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У цьому дослідженні розглядається вплив просторового положення локально захопленого заряду оксиду на ємності затвор–виток та затвор–сток SOI FinFET за допомогою тривимірного моделювання в TCAD Sentaurus. Результати показують, що розташування захопленого заряду сильно впливає на ємність затвор-витік через перерозподіл носіїв заряду поблизу поверхні каналу, тоді як спостерігається чітка реакція, коли захоплений заряд розташований поблизу краю оксиду. Більше того, співвідношення ємностей затвор-стік до затвор-витік систематично змінюється залежно від положення захопленого заряду вздовж каналу, що свідчить про те, що цей параметр може служити надійним електричним індикатором для виявлення захопленого заряду в оксиді та оцінки його просторового розподілу в FinFET-пристроях.

Ключові слова: *SOI FinFET; захоплений заряд в оксиді; ємність затвор-витік; ємність затвор-стік; розподіл заряду; TCAD-моделювання*