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STUDY OF THE INFLUENCE OF TEMPERATURE ON THE TRANSITIONS OF THE CdS/Si/CdTe HETEROSYSTEM

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The study presents the results of an investigation into the temperature dependence of the current–voltage characteristics of CdS/Si/CdTe heterostructures fabricated by thermal evaporation. The study establishes that, as the temperature increases, an exponential rise in current is observed, attributed to the thermally activated nature of conductivity and the reduction of the potential barrier at the interfacial boundaries. In the low-temperature region, the structure exhibits diode-like behavior, whereas at higher applied voltages (20–40 V), an injection transport mechanism becomes dominant. The activation energy of 0.61 eV confirms that the thermal release of carriers from localized states governs charge transport. The results indicate the stability of the barrier height and conduction mechanism over the studied temperature range, highlighting the need to account for thermal effects in the design of photoelectric and optoelectronic devices based on CdS/Si/CdTe structures.
Keywords: *Temperature; Heterosystem; Layer; Carrier; Mobility; Mechanism; Current; Voltage; Structure*
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INTRODUCTION

In recent years, there has been growing interest in the development and investigation of thin-film heterostructures based on group II–VI compounds, which are distinguished by their high photoelectric efficiency and thermal stability under operating conditions [1–3]. Among these materials, cadmium-containing compounds such as CdS and CdTe have attracted particular attention due to their direct bandgap nature, strong optical activity, and the technological simplicity of their deposition processes. These properties make them widely applicable in solar cells, photodetectors, and various optoelectronic devices [4–7]. The incorporation of a silicon layer into CdS/CdTe-based heterostructures enables more effective lattice parameter matching between the constituent layers, reduces defect density at the interfaces, and improves charge-carrier transport conditions, thereby enhancing the overall functional performance of the structure [8-10]. Such a heterostructure is considered a promising platform for developing photoconverters with a broad spectral sensitivity range. In this system, the CdS layer-a wide-bandgap semiconductor (E_g≈2.4 eV)-acts as a transparent window; silicon (E_g≈1.12 eV) serves as a buffer and transport layer; while CdTe-a narrow-bandgap semiconductor (E_g ≈ 1.5 eV)-provides efficient light absorption and charge-carrier generation [11,12]. The operational parameters of such structures are largely determined by temperature conditions, which influence the recombination rate, the potential barrier height of the p–n junction, and the carrier mobility.

The influence of temperature on the operating parameters of a photodiode is primarily determined by two fundamental diode characteristics-the ideality factor and the reverse saturation current density [13,14]. Direct-bandgap semiconductor materials such as CdS and CdTe have demonstrated high efficiency in the fabrication of thin-film photodiode structures [15,16].

To achieve the highest efficiency of photodiodes based on A^2B^6 compounds, the solid solution should possess a continuously graded composition across a thickness of d << 1 μm, ranging from CdS to CdTe [17]. The use of high-temperature processing during the formation of CdS/CdTe-based heterostructures incorporating a silicon layer leads to an increased concentration of uncontrolled impurities throughout the entire structure, including within the compound layers [18]. In CdS/CdTe heterostructures, a junction with pronounced rectifying behavior and high photosensitivity is typically formed [19, 20]. In addition to parameters such as layer thickness, doping level, bandgap width, charge-carrier mobility, and density of states, temperature effects exert a significant influence on the photoelectric characteristics and operational stability of photodiodes. Therefore, the investigation of the temperature dependence of current–voltage characteristics in CdS/Si/CdTe heterostructures represents a relevant and timely task aimed at optimizing their

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photoelectric properties and enhancing stability under various operating conditions. In the present study, the influence of temperature on the key operating parameters of CdS/Si/CdTe photodiode heterosystems was analyzed within the temperature range of 293–333 K. The results obtained provide insights into the temperature stability of these structures and contribute to the optimization of the performance characteristics of single- and multi-junction photodiodes, taking thermal effects into account.

EXPERIMENTAL PART

The investigated CdS/Si/CdTe heterosystem [21,22] was fabricated in a quasi-closed volume using the vacuum thermal evaporation method of CdS and CdTe powders onto an n-type monocrystalline silicon substrate. The substrate used was monocrystalline silicon of the KEF-600 grade, oriented along the (111) crystallographic direction, with a thickness of d=130 μm, a diameter of D=42 mm, and a specific resistivity of ρ=607.47 Ω·cm. The concentration of the majority charge carriers was $N_n=7\times10^{12}$ cm^{-3}, and the area of the resulting structure was 29 mm^2. The thickness of the deposited films was d = 0.55 μm and was determined using a MII-4 microinterferometer [21]. The films consist of microcrystalline blocks with a columnar grain structure, oriented along the growth direction and azimuthally disoriented. The grain sizes range from 50 to 100 μm, extending through the entire film thickness. This combination of structural parameters and technological conditions ensures the formation of a high-quality heterojunction with good crystallinity and minimal interfacial defects, which is a prerequisite for obtaining stable current–voltage characteristics of the photodiode over a wide temperature range [17].

The temperature dependence of the investigated photodiode samples of the CdS/Si/CdTe heterosystem was recorded in the measuring chamber of a Carl Zeiss Jena monochromator. The temperature regime in the investigated samples was set using a heater mounted in the sample holder placed inside the measuring chamber. The set temperature from room temperature to 60 ºC was measured with a copper-constantan thermocouple and maintained with a thermostat, as shown in Fig. 1.

The temperature in the studied sample 5 was controlled using a specially made low-inert heater – 4, mounted in the sample holder – 3, placed inside the measuring chamber. The temperature was set from room temperature to 60°C, with an accuracy of ±1°C It was measured by thermocouple 6 (chromel-droplet) and maintained by digital thermostat 2, taking into account the inertia of the system. Using a high-precision adjustable voltage source – 1, a fixed voltage was set, supplied to the studied sample – 5. From the output of the studied sample 5, the current flowing through the semiconductor structure was supplied to a digital current meter – 7, SH-300, used in the DC measurement mode.

Based on the obtained results, the dependence of current change on temperature was constructed using OriginPro 7.0.

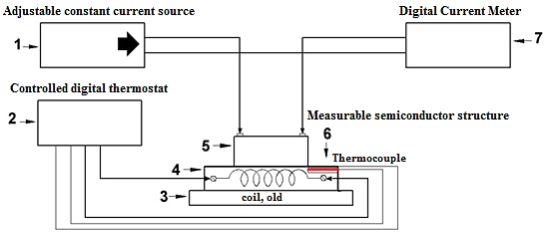


Figure 1. Block diagram for measuring the temperature dependence of the volt-ampere characteristic

RESULTS AND DISCUSSION

The current–voltage (I–V) characteristics of the structure were recorded in the forward direction over a wide range of current and voltage values. Assuming electrically active defects, analyzing I–V characteristics allows conclusions to be drawn about the defect structure formed within the heterosystem. Fig. 2 presents the forward branch of the I–V characteristic of the CdS/Si/CdTe heterosystem obtained at room temperature (293 K).

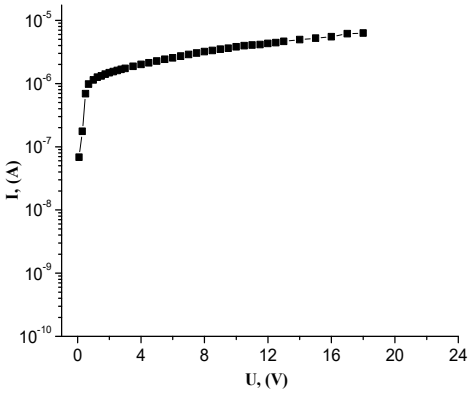


Figure 2. Volt-ampere characteristic of the CdS/Si/CdTe heterosystem in the forward direction at T=293 K

The current-voltage dependence is plotted on a semi-logarithmic scale. The analysis of the I-V characteristics indicates that the structure exhibits pronounced rectifying behavior. At 18 V, the rectification coefficient is ~10, confirming the diode-like behavior of the structure. Previously published research [23] presents the results of an analysis of the I-V characteristics of the CdS/Si/CdTe heterosystem.

The temperature dependence of the CdS/Si/CdTe heterosystem is shown in Fig. 3 and was recorded in the forward direction over wide current change ranges at fixed voltage. The study was conducted in the temperature range T=293÷333 K.

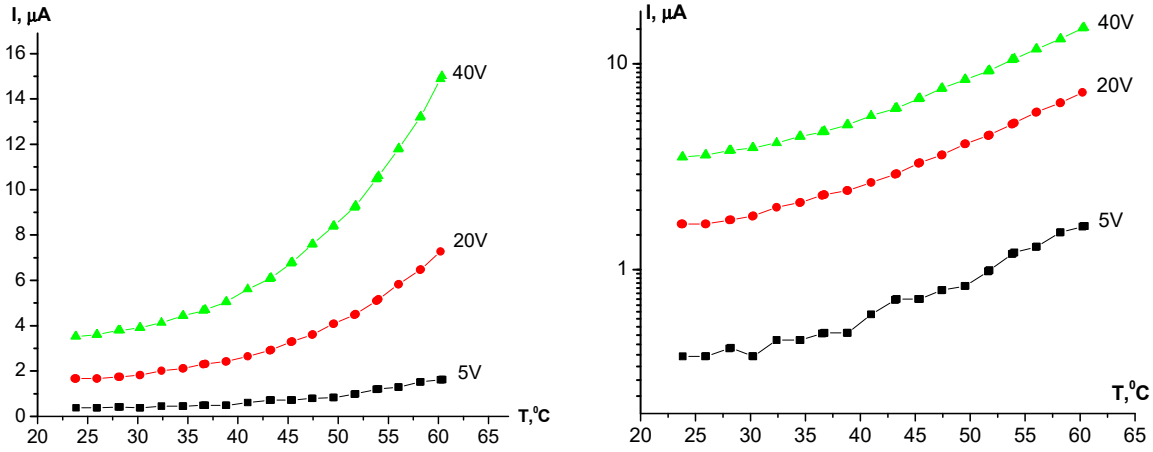


Figure 3. Current–voltage characteristics of the CdS/Si/CdTe heterosystem in the forward direction (a) and their sublinear regions (b) at fixed voltage values of 5 V, 20 V, and 40 V

In the obtained dependence (Fig. 3), an exponential increase in current with rising temperature was observed, indicating a thermally activated conduction mechanism. The forward branch of the I–V characteristics at low fixed voltages (5 V) followed an exponential dependence, whereas at higher voltages (up to 40 V) a sublinear increase in current with voltage was observed. In the low-temperature region, the current remained small due to the insufficient concentration of thermally excited carriers, while at low voltages (~5 V) an exponential current growth typical of diode structures with a diffusion-controlled conduction mechanism was evident. As the temperature increased, a noticeable enhancement of conductivity occured, associated with the intensification of thermal carrier generation and a reduction in the potential barrier at the CdS/Si and Si/CdTe heterointerfaces. At a fixed voltage of 20 V, the current increase was moderate, indicating a diode-type transition dominated by thermally activated charge transport processes. However, when the fixed voltage was increased to 40 V, the current rises much more rapidly, suggesting the onset of an injection-type conduction mechanism and an additional lowering of the barrier height at the heterojunction interface upon heating. An increase in temperature above 330 K was accompanied by a growth in leakage currents, which is likely associated with the thermal ionization of deep impurity and defect levels localized at the CdS/Si and Si/CdTe interfaces. The initial portion of the temperature dependence (Fig. 3) was well approximated by a known empirical law [24].

$$I = I_0 exp\ (eV/ckT) \tag{1}$$

The values of the exponent c in the exponent and the pre-exponential factor I_0, calculated from the temperature dependence (Fig. 3) for different temperatures, are given in Table 1.

Table 1. Values of the exponent c in the exponent and the pre-exponential factor I_0 at different temperatures

T, K	C	I_0, A
293	2.92	$5.17 \cdot 10^{-8}$
303	2.15	$8.02 \cdot 10^{-8}$
323	1.78	$2.53 \cdot 10^{-7}$
333	1.09	$3.02 \cdot 10^{-7}$

The transitions formed between the CdS/Si and Si/CdTe layers were high-resistance [25-27] and they mainly determined the electronic processes in the structure and the current transfer mechanism.

Dependence (1) is typical for the so-called “long” p-n diode, i.e. when $d/L_p>1$, where d is the base length, $L_p=(D_p\tau_p)^{1/2}$ is the diffusion length of minority carriers, D_p is the diffusion coefficient, τ_p is the lifetime of minority carriers. Since the electronic processes [28, 29] associated with charge modulation during current flow through the structure are largely determined by the transition high-resistance layers of CdS and CdTe, it is reasonable to take the thickness of these layers, which is approximately d≈0.55 μm, as the base length.

Exponential dependence of current on voltage (1) for p-i-n structures, the exponent c in the exponent has the following form:

$$c = \frac{2b+ch(d/L_p)+1}{b+1}, \quad (2)$$

where, $b=\mu_n/\mu_p$ is the ratio of electron and hole mobilities in the CdS/Si and Si/CdTe transition layers, b=9.12 [30, 31]. Knowing b, we can find $d/L_p=2.84$, then we can find the diffusion length of minority carriers: $L_p=0.71$ μm. This allowed us to determine the product of the mobility and the minority carrier lifetime $\mu_p\tau_p=qL^2_p/kT$, which was obtained at room temperature (293 K) as 1.38×10^{-7} см^2/V. At T=313 K, $\mu_p\tau_p=4.12\times10^{-7}$ см^2/V, which is e times greater than the value at room temperature; the increase in μpτp with temperature is explained by the recharging of deep centers.

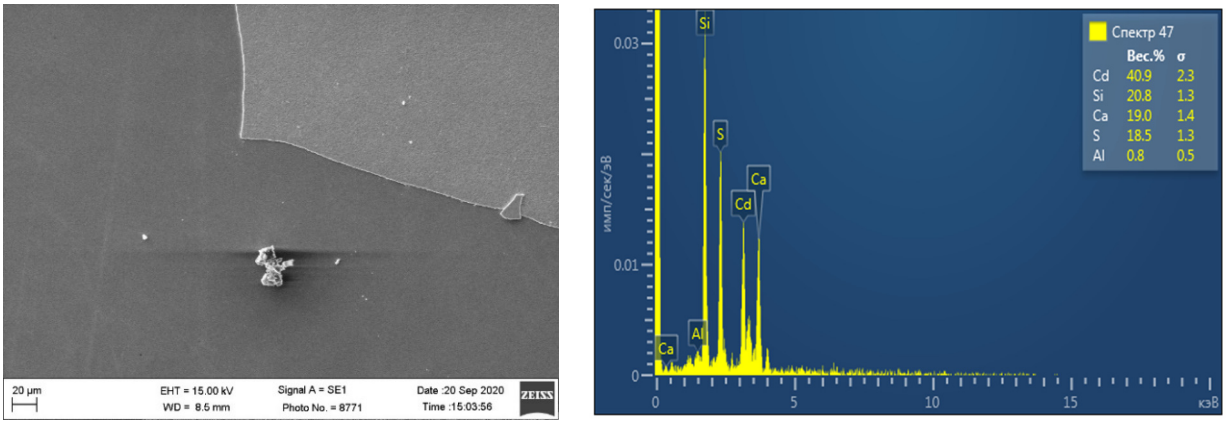
The minority carrier lifetime (τ_p) was determined by the relaxation process of nonequilibrium carriers at a low excitation level both in the mode without external voltage and at different values of the applied voltage [32, 33]. Nonequilibrium carriers were created using an electric pulse generated by a G5-63 rectangular pulse generator. The pulses had a sharp front and tail with a duration of 500-600 ns. The rise time did not exceed 3×10^{-9} s, and the duty cycle was at least 6×10^{-4} s. In the absence of external voltage, the change in the concentration of nonequilibrium carriers n over time is described by an exponential dependence:

$$\Delta n = \Delta n_0 exp(-t/\tau), \quad (3)$$

where, t is the time and τ is the relaxation time constant. Based on dependence (5), the value of this constant was obtained: $\tau\approx3.16\times10^{-7}$ s. Since in the structures under consideration the relaxation process was determined by the modulation of currents by minority carriers, the characteristic relaxation time corresponds to the lifetime of minority carriers, i.e. $\tau_p\approx3.16\times10^{-7}$ s.

To avoid losses caused by the voltage drop in the bulk of the CdTe film, the Fermi level should be no further than approximately 0.2 eV from the upper boundary of the valence band, and for CdS, no further than 0.08 eV from the conduction band. The situation was complicated by the fact that even ultrapure CdTe and CdS samples inevitably contain residual impurities such as Cu, Fe, Au, Ag, As, P, and others in concentrations reached 10^{15}-10^{16} cm^{-3} [34-35]. In addition to uncontrolled impurities, electrically active defects arised in the material, which were formed during its synthesis, as well as during mechanical or chemical treatment. For example, Cd vacancies are capable of forming singly or doubly charged acceptor states, and in combination with impurities such as Cl, they form donor complexes (known as A-centers). Te vacancies and Te atoms in interstitial sites or at Cd sites also behaved similarly to impurities of various natures. As a result, both shallow and deep acceptor and donor levels were inevitably present in the CdTe band gap, making this material a partially compensated semiconductor [36].

Fig. 4 shows SEM images of a thin-base CdS film grown on a silicon substrate of n-type CdS/Si/CdTe heterosystem and mass fractions of cadmium (Cd) elements and residual impurities in percentage. It can also be seen that the back side of the sample, consisting of silicon, is partially covered with a thin CdS film.



a b

Figure 4. SEM images of the surface (a) and elemental analysis (b) of a thin base layer based on n-type CdS of the CdS/Si/CdTe heterosystem

It is known that, in the general case, the current–voltage characteristic (I–V characteristic) of a p–n junction under forward bias can be expressed by the following formula [24]:

$$I = I_s exp\frac{qV}{nkT}, \quad (4)$$

determine the voltage drop across the p-n junction, which has the following expression:

$$V = \frac{nkT}{q} ln\frac{I}{I_s}, \quad (5)$$

According to the dependencies (Fig. 5) measured on experimental samples at different temperatures, it was noted that with a change in temperature, the coefficient of non-ideality also changed. In this case, the coefficient of non-ideality changes linearly inversely proportional to the temperature (1/T) and is expressed as follows:

$$n = n_0 + \frac{T_0}{T} \tag{6}$$

where, n_0 and T_0 are constants of the empirical formula describing the dependence of the non-ideality coefficient on temperature. For the experimental samples under study at T_0=310 K, the value of n_0 is 0.72.

In practical calculations, the ideality factor is determined from the slope of the linear section of the I–V characteristic (Fig. 5) in semilogarithmic coordinates using the following expression:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln(I_S))}\right) \tag{7}$$

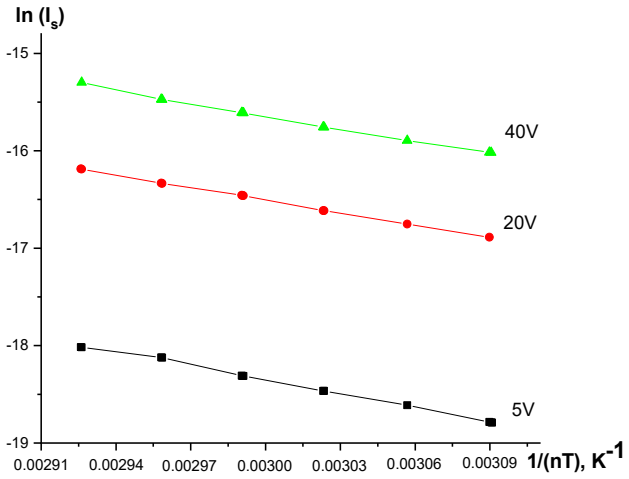


Figure 5. Arrhenius dependence of the pre-exponential factor for the CdS/Si/CdTe heterosystem

The graph shown in Fig. 5 illustrates the dependence of the logarithm of the saturation current ($\ln I_s$) on the inverse temperature (1/(nT)) for the CdS/Si/CdTe heterosystem at various fixed voltages: 5 V, 20 V, and 40 V. The linear nature of the dependencies corresponding to voltages of 20 V and 40 V indicates a thermally activated mechanism of saturation current conduction, which follows an exponential relationship described by expression (8) [24, 37].

$$I_s = I_{s0} exp\ (-\frac{\Delta E}{nkT}), \tag{8}$$

where, ΔE - activation energy, k is the Boltzmann constant, T is the absolute temperature, and n is the ideality factor of the junction.

The negative slope of the temperature dependences of the logarithm of the saturation current indicates an increase in current with rising temperature (decreasing 1/(nT)), which is characteristic of diode structures where charge transport occurs via thermoelectronic emission across the potential barrier. The parallelism of the lines corresponding to different applied voltage values indicates that the activation energy remains constant within the studied temperature range, confirming the stability of the barrier height and the preservation of the charge transport mechanism [23,38]. At higher fixed voltages, an increase in the saturation current values is observed, which is associated with a reduction in the effective potential barrier height and an enhancement of injection processes in the heterojunction region. The linear dependence:

$$\ln(I_s) = f(1/nT) \tag{9}$$

confirms the thermally activated nature of the saturation current and allows for the evaluation of the energy parameters of the barrier junction in the CdS/Si/CdTe structure.

From the temperature dependence (Fig. 5) of the CdS/Si/CdTe heterosystem, the activation energy of charge carriers was estimated to be $\Delta E \approx 0.61$ eV, while the saturation current at the junctions was $I_{s0}=6.3\times10^{-8}$ A. The obtained activation energy value indicates a thermally activated conduction mechanism, in which charge transport is governed by the thermal release of carriers from localized energy states or by their overcoming of the potential barrier at the heterojunction interface. Based on the dependence shown in Fig. 5 and according to expression (7), the ideality factor was calculated to be n=3.6, which indicates a combined current transport mechanism in the CdS/Si/CdTe heterosystem [39,15]. Along with the diffusion transport of charge carriers, recombination and injection processes make a significant contribution to conductivity, as well as the influence of localized energy states and the inhomogeneity of the potential barrier at the interfacial boundaries [15].

According to the literature [24], the specific resistance of the material at a given temperature is determined by the concentration of the majority charge carriers (n) according to the expression $\rho=1/q\mu_n n$. In the CdS/Si/CdTe heterosystem at room temperature (293 K), the carrier concentration is about 10^{11} cm^{-3} and increases with increasing temperature, reaching up to 2×10^{12} cm^{-3} at 333 K. This indicates that the studied structure is a highly compensated material in which the concentration of ionized defect complexes of the ($V^{-2}_{Cd}D^{+}$) - type is about 10^{11} cm^{-3} at room temperature.

CONCLUSIONS

The conducted studies have shown that temperature has a significant effect on the I–V characteristics of the CdS/Si/CdTe heterosystem. With increasing temperature, an exponential rise in current was observed, which is attributed to the thermally activated nature of conductivity and the reduction of the potential barrier at the interfacial boundaries. In the low-temperature region, the current remained small, whereas at low voltages (~5 V) the structure exhibited diode-like behavior characteristic of a diffusion-controlled carrier transport mechanism. When the applied voltage was increased to 40 V, an injection-type conduction mechanism stayed dominant, caused by a reduction in the barrier height upon heating. The observed increase in current with temperature indicates a decrease in the effective barrier height, confirming the stability of the electronic properties of the junction within the investigated temperature range.

The study of the temperature dependence in the sublinear region revealed that the deep energy levels within the structure are continuously distributed, with their concentration increasing toward the mid-gap region. It was established that the μpτp parameter in the heterosystem increases with temperature: at T=293 K, $\mu_p\tau_p=1.38\times10^{-7}$ см^2/V, while at T=313 K, $\mu_p\tau_p=4.12\times10^{-7}$ см^2/V. Based on the measured specific resistivity of the heterostructure at the corresponding temperatures, the concentration of the majority charge carriers was determined to be approximately $10^{11}cm^{-3}$, increasing to about 2×10^{11} cm^{-3} with rising temperature.

The temperature dependence of the pre-exponential factor I_0 in the exponential region of the current–voltage characteristics indicates a complex variation in the equilibrium charge carrier concentration within the CdS/Si/CdTe heterosystem. This behavior is attributed to the influence of deep energy levels, recombination centers, and the potential distribution features at the interfacial boundaries. It has been established that the conduction process in the CdS/Si/CdTe heterosystem exhibits a thermoactivated character. The activation energy of 0.61 eV suggests that charge transport was governed by the thermal release of carriers from localized states or by their surmounting of the potential barrier at the heterojunction interface.

The obtained results confirm the stability of the barrier height and the invariance of the carrier transport mechanism within the investigated temperature range, while also demonstrating the enhancement of injection processes under higher applied voltages. The revealed regularities highlight the necessity of accounting for temperature effects in the design and operation of photoelectric and optoelectronic devices based on CdS/Si/CdTe structures. The findings can be utilized to optimize the parameters of photoconverters and optical memory devices operating over a wide temperature range.

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ДОСЛІДЖЕННЯ ВПЛИВУ ТЕМПЕРАТУРИ НА ПЕРЕХОДИ ГЕТЕРОСИСТЕМИ CdS/Si/CdTe

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У дослідженні представлені результати дослідження температурної залежності вольт-амперних характеристик гетероструктур CdS/Si/CdTe, виготовлених методом термічного випаровування. Встановлено, що зі збільшенням температури спостерігається експоненціальне збільшення струму, що пояснюється термоактивованою природою провідності та зменшенням потенційного бар'єру на міжфазних межах. В області низьких температур структура демонструє діодоподібну поведінку, тоді як при вищих прикладених напругах (20–40 В) домінує інжекційний механізм транспорту. Енергія активації 0,61 еВ підтверджує, що теплове вивільнення носіїв заряду з локалізованих станів керує транспортом заряду. Отримані результати свідчать про стабільність висоти бар'єру та механізму провідності в досліджуваному діапазоні температур, а також про необхідність врахування теплових ефектів при проектуванні фотоелектричних та оптоелектронних пристроїв на основі структур CdS/Si/CdTe.

Ключові слова: *температура; гетеросистема; шар; носій; рухливість; механізм; струм; напруга; структура*