EAST EUROPEAN JOURNAL OF PHYSICS. 3. 325-335 (2025)
DOI:10.26565/2312-4334-2025-3-31 ISSN 2312-4334

CURRENT TRANSFER MECHANISM IN A THIN-BASED HETEROSYSTEM BASED ON A^2B^6 COMPOUNDS

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Received June 4, 2025; revised July 28, 2025; accepted July 31, 2025

The possibility of fabricating a heterosystem based on A^2B^6 compounds with potential barriers (Au)CdS/Si/CdTe(Au) with a minimum density of surface states is presented, confirmed by measurements of the potential barrier height based on capacitance-voltage methods. Various exponential dependences of the current on the voltage at forward biases associated with a change in the kinetic parameters of the CdS/Si/CdTe structure base are determined, and it is revealed that at current densities of $2.1\times10^{-7} \div 0.35\times10^{-6}$ A/cm^{-2} in the studied CdS/Si/CdTe structure, the current is limited by recombination in the space charge layer. It is shown that when a reverse bias is applied to the structure, the structure base is completely covered by the space charge accompanied by electron injection from the rear contact, which in turn determines the mechanism of current transfer of the structure.
Keywords: *Heterosystem; Deposition; Base; Layer; Barrier; Photodiode; Current density; Capacity; SEM, Band diagram*
PACS: 64.70.kg, 73.40.Kp, 68.37.Hk

INTRODUCTION

The prospect of using phenomena occurring in the volume of a semiconductor to increase the functional capabilities, improve the reliability of semiconductor and microelectronic devices and expand the ranges of their operating frequencies and powers allows for a significant simplification of the technology of semiconductor instrument making [1]. In recent years, there has been particular research interest in the creation of heterojunctions based on A^2B^6 compounds, in particular based on cadmium sulfide and telluride. Heterostructures based on these materials are proposed as photoelectric converters of solar energy [2-4], photodetectors [5-7], and detectors [8-11, 28].

However, for high-quality optoelectronic devices (photodetectors), such heterojunctions are combined with silicon in the CdTe-Si and CdS-Si systems. These heterojunctions are difficult to manufacture, since the crystal lattice parameters of CdS, CdTe and Si differ by 15%, which leads to the formation of a high density of surface defects at the Si-CdTe, Si-CdS interfaces. Nevertheless, the possibility of obtaining high-quality Si-CdTe-CdS heterojunctions with low surface density by forming an intermediate transition layer that acts as a buffer in the nSi-pCdTe, pCdTe-nCdS, CdTe-Si structure has been demonstrated in [12, 13].

For A^2B^6 semiconductors, including CdS and CdTe, it is technologically difficult to obtain a p-i-n structure on its basis due to the self-compensation effect. As is known, when manufacturing heterojunctions, a high-resistance i-layer is often formed at the heterointerface due to mutual diffusion of atoms of one semiconductor into another [14, 32]. To avoid this problem, we created a two-side sensitive thin-base structure (Au)CdS/Si/CdTe(Au) with heterojunctions grown by compositionally differentiated layers of CdTe and CdS on n-type Si substrates, with certain layer compositions depending on their thickness. It is well known that thin films of CdTe and CdS can be grown on various substrates using different methods [15,16]. Basically, such films are obtained by thermal deposition in vacuum, that is, by growing from the vapor phase [17].

In this work, CdTe and CdS layers were grown using this method because it allows obtaining various photosensitive structures with fast response.

There is no information in the sources about the creation of two-way sensitive photodiodes with CdS/Si/CdTe with a heterosystem with internal amplification, which are tuned to the required wavelengths of optical radiation by external action, i.e. with different supply of bias voltage. Their production is a topical task, since such a photodiode replaces several photodetectors that are sensitive in different regions of the wavelength of optical radiation and are rigidly connected with the width of the forbidden zone. In the CdS/Si/CdTe semiconductor system, the counter currents of nonequilibrium carriers are regulated, due to which the inversion of the sign of photosensitivity occurs at different base thicknesses [18, 19]. This paper presents the results of studies to identify the role of high-resistance and low-resistance heterolayers in the current transfer mechanism in the CdS/Si/CdTe heterosystem by studying the electrophysical characteristics of heterosystems.

Cite as: Sh.B. Utamuradova, F.A. Giyasova, K.N. Bakhronov, M.A. Yuldoshev, M.R. Bekchanova, B. Ismatov, East Eur. J. Phys. 3, 325 (2025), https://doi.org/10.26565/2312-4334-2025-3-31
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EXPERIMENTAL PART

The investigated heterosystem CdS/Si/CdTe photodiode structure [20, 28] was fabricated by successive vacuum thermal evaporation [21] of CdS and CdTe powders onto a substrate - the surface of a wafer of single-crystal n-type silicon. During deposition of the CdS film onto the surface of the silicon substrate, the evaporator temperature was 850÷950°C, which is necessary for congruent evaporation of CdS particles, and a CdTe film was deposited on the back side of the substrate at an evaporator temperature of 580 °C. During film deposition, the substrate temperature was 270÷290°C, the film growth time was 5 min. at a rate of 16.7 Å/s, at which the thickness of each film was 0.55 µm. To obtain a rectifying contact on the surface of the film layers of the heterosystem, metal-semiconductor junctions made of Au with a thickness of 70 Å were formed in the vacuum post VUP-4 at a temperature of 435°C. The contact area of Au on the surface is 0.29 cm^2. The technological route for manufacturing the heterosystem is given in [22, 23]. The manufactured structure of a photodiode based on the CdS/Si/CdTe heterosystem with contacts made of Au is shown in Fig. 1.

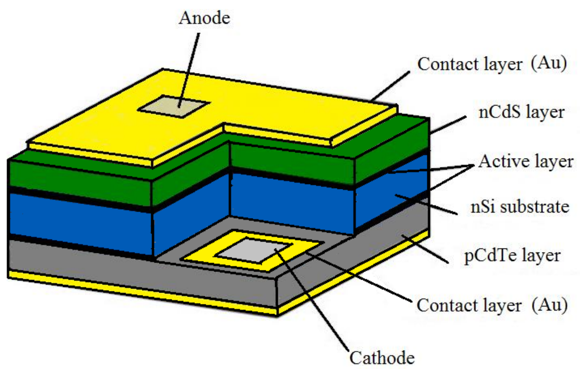
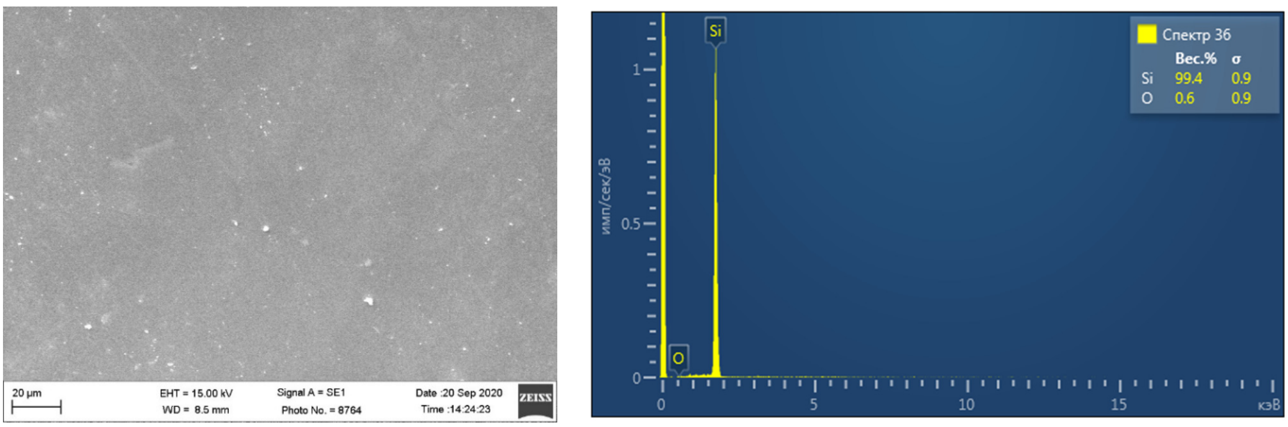


Figure 1. Design of a lateral bidirectional photodiode based on (Au)CdS/Si/CdTe(Au)

ELEMENTAL ANALYSIS OF SAMPLES

The morphology of the CdS/Si/CdTe heterostructure samples based on silicon substrates was studied using a scanning electron microscope SEM EVO MA 10 (Carl Zeiss, Germany). The elemental composition was studied using an energy-dispersive analyzer EDX (Oxford Instruments) - Aztec Energy Advanced X-act SDD. During the measurements, an accelerating voltage of 15 kV was applied to the filament of the device, while the working distance from the structure was 8.5 mm.

Fig. 2-4 show the surface morphology of a sample of a two-side sensitive CdS/Si/CdTe heterosystem. Measurements were carried out on both sides of the heterostructure.

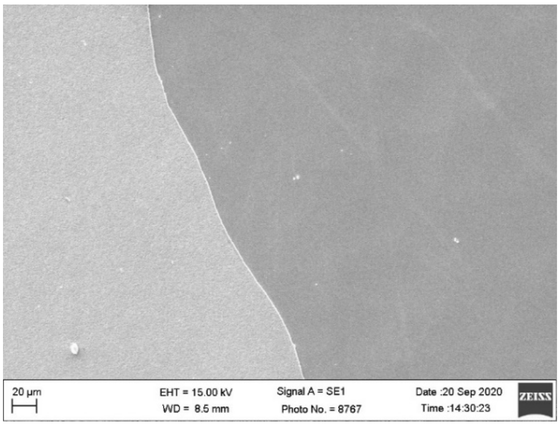


a **b**

Figure 2. SEM images of the surface (a) and elemental analysis (b) of single-crystal n-type silicon heterostructure CdS/Si/CdTe

The results of the scanning electron microscope (SEM) analysis, presented in Figure 2, confirm that silicon is the predominant element in the sample composition, as evidenced by the intensity of its main peak. The presence of low-intensity oxygen peak (O) indicates the formation of oxide compounds or surface contamination, which may have occurred during sample growth or storage. Quantitative analysis shows that the mass fraction of silicon is 99.4%, oxygen – 0.6%.

Fig. 3 shows an image of a thin-base CdS film grown on a silicon substrate of an n-type heterostructure. According to the quantitative analysis, it is clear that the mass fraction of cadmium (Cd) is 52.9%, sulfur (S) is 15.1%, silicon (Si) is 32.1% and, accordingly, the amount of Cd significantly exceeds the amount of S. However, point defects can form near the boundary of Si and CdS [24,25].



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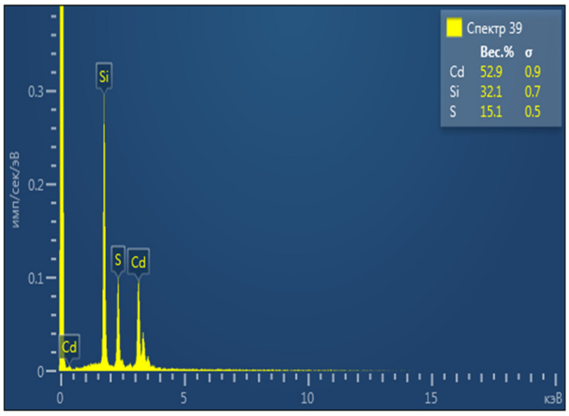

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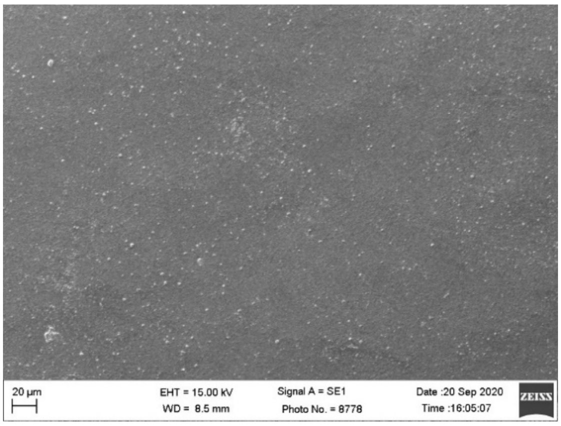
Figure 3. SEM images of the surface (a) and elemental analysis (b) of a thin base layer based on CdS of the n-type CdS/Si/CdTe heterostructure

Fig. 4 shows an image of a thin-based CdTe film grown on a silicon substrate of an n-type heterostructure. The mass fractions of cadmium (Cd) and tellurium (Te) are 47.8% and 52.2%, respectively, the amounts of these elements are almost identical. It can also be seen that the back side of the sample, consisting of silicon, is completely covered with a thin CdTe film, as evidenced by the absence of Si in the spectra.



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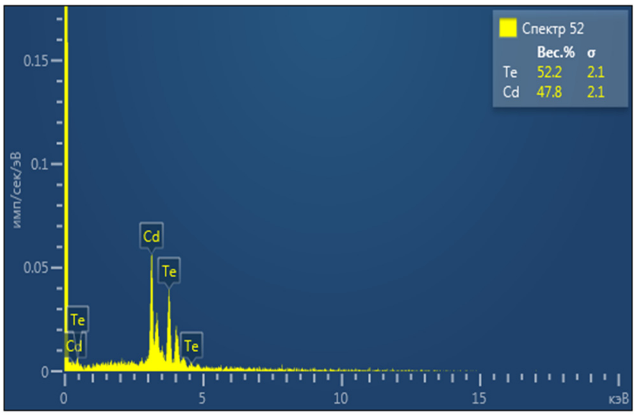

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Figure 4. SEM images of the surface (a) and elemental analysis (b) of a thin base layer based on CdTe p-type heterostructure CdS/Si/CdTe

The CdS/Si/CdTe heterosystem structures obtained by vacuum thermal evaporation in a quasi-closed volume are a simple, effective and inexpensive method for microelectronic devices. However, intensive research is required to fully reveal its potential. The presented results demonstrate compactness, the ability to grow in one direction and obtain rod- or columnar-type grains with normal properties for growing substrates [26,27].

The current-voltage characteristics (CVC) of the manufactured CdS/Si/CdTe photodiode heterosystem were measured with forward and reverse current directions in the dark and in the light at room temperature. The operating voltage was supplied from a B5-48 and B5-50 power supply with a step of 0.05 volts. The voltage and current were recorded with a B7-21A and B7-35 universal voltmeter. The minimum current was 2 nA, the relative measurement error was 0.2÷0.4%. The structures were illuminated with a JDSU850 laser with a radiation power of 2.3 W and a wavelength of 850 µm, as well as with a SIRSh 6-100 incandescent lamp with a power of N=100 W, which in its parameters is identical to the reference white light lamp [23]. In such a lamp, the power of electromagnetic radiation in the visible spectrum in one lumen is 9.1×10^{-3} W [28].

The capacitance-voltage characteristics of the studied CdS/Si/CdTe heterosystems were measured with a capacitance value within the range of (0.1÷50 nF) at a room temperature of 300 K in the forward and reverse switching modes in the frequency range f=0.4÷50 kHz, since in this frequency range they are identical in shape. A detailed description of the CVC measurement technique for the studied structure is given in [23].

RESULTS AND DISCUSSION

Establishing the patterns and processes of current flow through homo- and heterojunction structures is the initial stage of studying semiconductor devices based on them. Under the condition of electrical activity of defects, the analysis of the current-voltage characteristics allows us to draw conclusions about the defectiveness of the heterostructures formed [29].

Fig. 5 shows the forward and reverse branches of the CVC of the CdS/Si/CdTe heterosystem with potential barriers. The dependence is plotted on a semi-logarithmic scale. The conducted analysis of the CVC indicates that the structure has pronounced rectifying properties. At a voltage of 18 V, the rectification coefficient is ~ 10, which confirms the presence of diode-like behavior of the structure [30, 31].

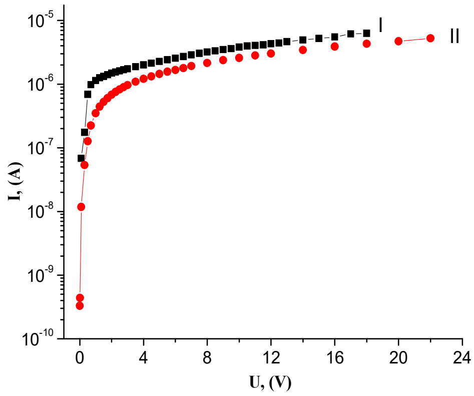


Figure 5. Forward (I) and reverse (II) branches of the CVC of the CdS/Si/CdTe heterosystem with potential barriers at t=20 °C

Analysis of the direct branch of the CdS/Si/CdTe heterosystem current-voltage characteristic shows that the curve consists of four characteristic sections (Fig. 6). Each of the sections: the first, second, third and fourth – is described by an exponential dependence of the current on the applied voltage and is represented by an analytical equation [32]:

$$I = I_0[\exp(qV/ckT)-1] \tag{1}$$

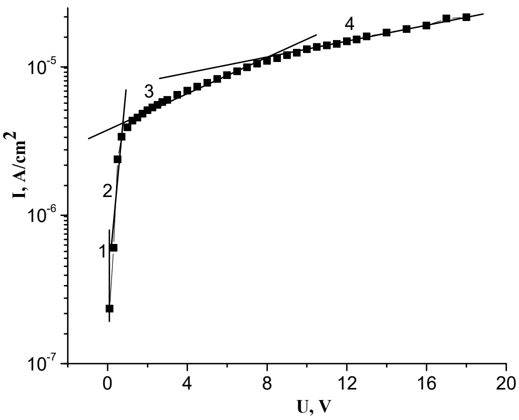


Figure 6. Direct branch of the CdS/Si/CdTe heterosystem with potential barriers on a semi-logarithmic scale in the dark

As can be seen in Fig. 6, in the first section of the direct branch of the I-V characteristic at a current density within the range of $I \approx 2.02\times10^{-8} \div 0.52\times10^{-7}$ A/cm², an exponential dependence is observed with the exponent $c_1 = 1.028$ and the pre-exponential factor $I_{01} = 2.2\times10^{-7}$ A/cm². The current flowing in this section of the structure is caused by thermionic emission [32]. Such a current transfer mechanism is typical for structures with a Schottky barrier and metal-insulator junctions. The thermionic current is described by the following equation [33, 39]:

$$I_{01} = AT^2\exp(-V_D/kT) \tag{2}$$

Using the experimentally determined value of the pre-exponential factor $I_{01} = 2.2\times10^{-7}$ A/cm², obtained from the analysis of the first section of the I-V characteristic based on expression (2), the value of the potential barrier height was calculated: $V_D = 0.843 \pm 0.02$ eV. The obtained value is in good agreement with the barrier value determined from the results of the I-V characteristic given below. From the given data, it can be said that in the first section of the direct branch of the I-V characteristic, the main current mechanism is thermionic emission, which is caused by the emission of electrons from the gold contact Au into the CdTe (or CdS) layers.

In the second section of the current-voltage characteristic, at current densities $I = 2.1\times10^{-7} \div 0.35\times10^{-6}$ A/cm² for the Si/CdTe heterojunction, the dependence of the current on the voltage is also exponential. In this case, the exponent is $c_2 = 1.98$, and the pre-exponential factor is $I_{02} = 6.1\times10^{-7}$ A/cm² (Fig. 6, straight line 2).

The value $c_2 \approx 2$ indicates that the current in this mode is limited by carrier recombination in the space charge layer [34]. In wide-gap semiconductors, especially at low temperatures, recombination processes have a significant effect on the shape of the current-voltage characteristic even at forward voltage.

The carrier concentration, including nonequilibrium, in the space charge layer changes by a factor of e over a characteristic distance l, at which the potential changes by kT/q. At a low injection level, the recombination rate is determined by the product of the electron and hole concentrations, and maximum recombination occurs at the boundary of the p- and n-regions.

Calculations show that the bulk of carriers in the space charge layer recombine into a layer less than 0.55 μm thick, located near the geometric boundary of the CdTe (Au) potential barrier. The expression $l=kT/qE_{max}$ is used to determine the diffusion displacement length in neutral regions. For the structure under study, the maximum electric field strength is 5.23×10^2 V/cm [32]. Recombination processes are especially noticeable in semiconductors containing metastable complexes [35]. Similar patterns are observed in A^2B^6 compounds, where excitation causes chemical reactions that lead to the disintegration of complex complexes, such as a shallow donor – vacancy [36]. Despite the differences in the mechanisms, the following remains common to all cases: the recombination of nonequilibrium carriers occurs with a delay, and the inertia of the electron exchange within the recombination complex leads to the appearance of an additional term in the denominator of formula (3), which, at a high level of excitation, can become the dominant factor [37, 38].

$$U = N_R \frac{c_n c_p (pn - n_i^2)}{c_n(n+n_1) + c_p(p+p_1) + a\tau_i pn}\,. \quad (3)$$

Since at sufficiently high values of forward voltage the recombination current increases with increasing bias more slowly than the diffusion current, the main contribution to the current begins to be made by carrier diffusion in the quasi-neutral regions of the base. In such a situation, the applied voltage is redistributed between the potential barrier and the quasi-neutral part of the base, which is reflected in the value of the exponent c in the I-V equation. The value of the exponential factor depends on the ratio of the base thickness to the diffusion length of minority carriers. For different ratios of these parameters, the exponent can take different values, which allows us to judge the dominant mechanism of current transfer in the heterosystem.

In Fig. 6, sections 3 and 4 of the I-V characteristics are described by the dependence: I=exp(qV/ckT), where the values of the exponent c significantly exceed 2 and are 12.7 for section 3, and 48.3 for section 4, and the pre-exponential factors are 4.4×10^{-6} A/cm² and 1.1×10^{-5} A/cm², respectively. Such high values of c indicate the presence of complex recombination processes occurring through several channels. This indicates that at a given injection level, certain types of recombination centers participate in recombination, probably representing complex formations in which carriers are retained for a certain time. Such a model is valid for a high-resistance compensated base of the Si/CdTe heterosystem. Electrons are injected into the quasi-neutral part of the CdS/Si base from the metal contact (Au)CdS, and the resistance of this contact makes a significant contribution to the shape of the I–V characteristic [39].

It is worth noting that no holes are injected from the CdS/Si heterojunction into the base, as shown in [34], since this effect is characteristic only of ideal heterojunctions. In real conditions, surface states at the interface of semiconductors can act as recombination or tunneling centers for holes.

Based on the above, the main contribution to the structure current is made by the flow of electrons injected from the (Au)CdS contact. At the same time, as the analysis of the second section of the I-V characteristic shows, diffusion currents flow in the base, caused by non-main nonequilibrium holes coming from the Si/CdTe heterojunction to compensate for the charge and ensure the electrical neutrality of the injected electrons.

According to literature data [40], with an insignificant accumulation effect, in the diffusion mode only two characteristic types of current-voltage dependences can be realized: I∼exp(qV/kT) and I∼exp(qV/ckT).

Under forward bias near the CdTe(Au) contact, electrons and holes accumulate to maintain electroneutrality. This is due to the presence of a high potential barrier of 0.843 eV, which promotes the accumulation of nonequilibrium charge carriers and the formation of a positive concentration gradient: dn/dx>0. As a result, diffusion and drift carrier flows directed in opposite directions arise in this region. Upon reaching a certain bias level (about 1.5 V), these flows mutually compensate, which leads to an increase in the base resistance and the appearance of a sublinear dependence of current on voltage [28, 41].

The CdS/Si/CdTe heterosystem may contain point defects, such as cadmium (Cd), sulfur (S) or tellurium (Te) atom vacancies. Despite the difference in composition and type, the recombination of nonequilibrium electrons and holes in the structure occurs with a delay. This behavior is due to the inertia of the electron exchange inside the recombination complex, which manifests itself at a sufficiently high excitation level. This inertia leads to a recombination delay, which must be taken into account when analyzing the dynamic characteristics of the structure.

As is known, in CdTe and CdS compounds, cadmium atoms are volatile components, as a result of which cadmium atom vacancies are easily formed in their crystal lattice: both singly charged V_{Cd}^{-} and doubly charged V_{Cd}^{2-}, and the appearance of interstitial cadmium atoms (Cd_i) is also possible. [41-43]. These complexes represent deep acceptor levels, similar to gold atoms, and probably play an important role in recombination processes. There is a high probability that such defect-impurity formations form recombination complexes of the type: negatively charged acceptor - positively charged interstitial ion, positively charged donor - negatively charged vacancy [44, 45]. Recombination of nonequilibrium charge carriers through such complexes occurs with a characteristic delay due to the inertia of the electron exchange inside the complex. At high current densities, it is these processes that become dominant in recombination, especially in Si/CdTe base layers.

As a rule, the height of the potential barrier at the metal-semiconductor interface is determined by the difference in the work function between the metal and the semiconductor. According to [29], the work function of gold (Au) is in the range of 4.0÷5.2 eV, and its exact value largely depends on the state of the metal surface.

Next, we will analyze the behavior of the reverse branch of the CdS/Si/CdTe heterosystem's I–V characteristic (Fig. 7).

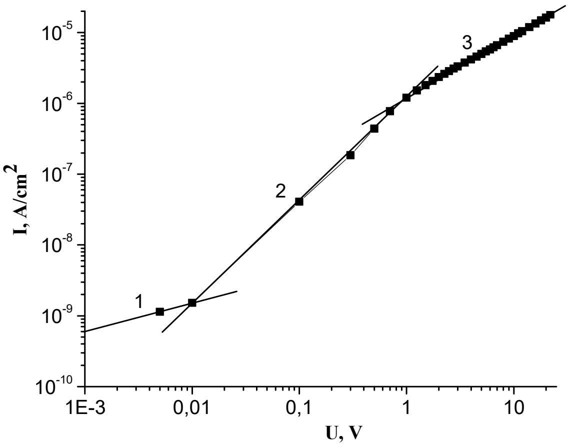


Figure 7. I-V characteristics of the reverse-biased CdS/Si/CdTe heterosystem in double logarithmic scale

The geometric parameters of the space charge region, in particular its thickness, as well as leakage currents through the rectifying contact and the characteristics of the ohmic contact, have a significant effect on the formation of the spectrometric parameters of the photodiode [46]. In this regard, it is of interest to study the electronic processes occurring in the space charge layers formed in the base layers of the CdS/Si/CdTe heterosystem with potential barriers. An important task of the study is to study the influence of the properties of the rear ohmic contacts on the nature and intensity of these processes, since they also significantly affect the overall efficiency and stability of the photodiode structures [47].

Analyzing the reverse branch of the current-voltage characteristic (Fig. 7) by power dependences of the type - $I=AV^{\alpha}$ with different values of the exponent α, at room temperature, we have three clearly defined sections: in the voltage range from 0 to 0.01 V – $J \propto V^{0.78}$ (recombination process) in section 1, in the range from 0.02 V to 3 V – $J \propto V^{2.44}$ (injection depletion effect) in section 2, in the range from 4 to 13 V – $J \propto V^{5.55}$ (pre-breakdown) in section 3.

According to the theory [48], diode structures have a power-law dependence of current on voltage of the type $J \propto V^{\alpha}$, ($\alpha \geq 2$), including a section of sharp current growth when, in addition to point defects, complex defect-impurity complexes participate in recombination processes, within which electron exchange occurs, determined by formula (3).

According to the theory presented in [41], in structures with developed accumulation, the sublinear section of the I–V characteristic appears when the conditions Jad≥2 is met. This shows that for samples of structures based on CdS/Si/CdTe, the value of Jad=3 at T=300 K.

This section of the I–V characteristic can be well described within the framework of the above-described theory of the injection depletion effect [40]:

$$V = V_0 \, exp(\, aJd) \tag{4}$$

where, $a = \frac{1}{2kT\mu_n N_t}$ is a parameter that depends only on the mobility of the majority carriers – electrons (μ_n) and the concentration of deep impurities – N_t. Using expression (4), the value of the parameter "a" can be determined directly from the sublinear section of the current-voltage characteristic, as shown in Fig. 5. With forward and reverse bias on a logarithmic scale:

$$a = \frac{S \cdot ln(V_2/V_1)}{(I_2 - I_1) \cdot d}, \tag{5}$$

The value of the parameter "a" in expression (5), determined on the basis of the experimental data of the CdS/Si/CdTe structure I–V characteristics, was at room temperature $a=5.22\times10^4$ cm/A, then, accordingly, $\mu_n \times N_t = 2.31\times10^{15}$ $V^{-1}\cdot cm^{-1}\cdot s^{-1}$. The mobility of the majority carriers was $\mu_n \approx 500$ $cm^2/V\cdot s$, and that of the minority carriers $\mu_p \approx 60$ $cm^2/V\cdot s$, therefore, the concentration of deep impurities leading to the appearance of the injection depletion effect was $N_t \approx 4.62\times10^{12}$ cm^{-3} [30,31].

In section 1 of the current-voltage characteristic, the dependence of the current on the voltage is close to $I \sim V^{1/2}$. Such a dependence is typical for cases when, with an increase in the reverse bias, the expansion of the volume charge region occurs [36]. When the diode operates with potential barriers in the reverse direction, the reverse current density can be described by the following expression [34]:

$$I_0 = qL_n(n_p/\tau_n) + qd(n_i/2\tau_0), \tag{6}$$

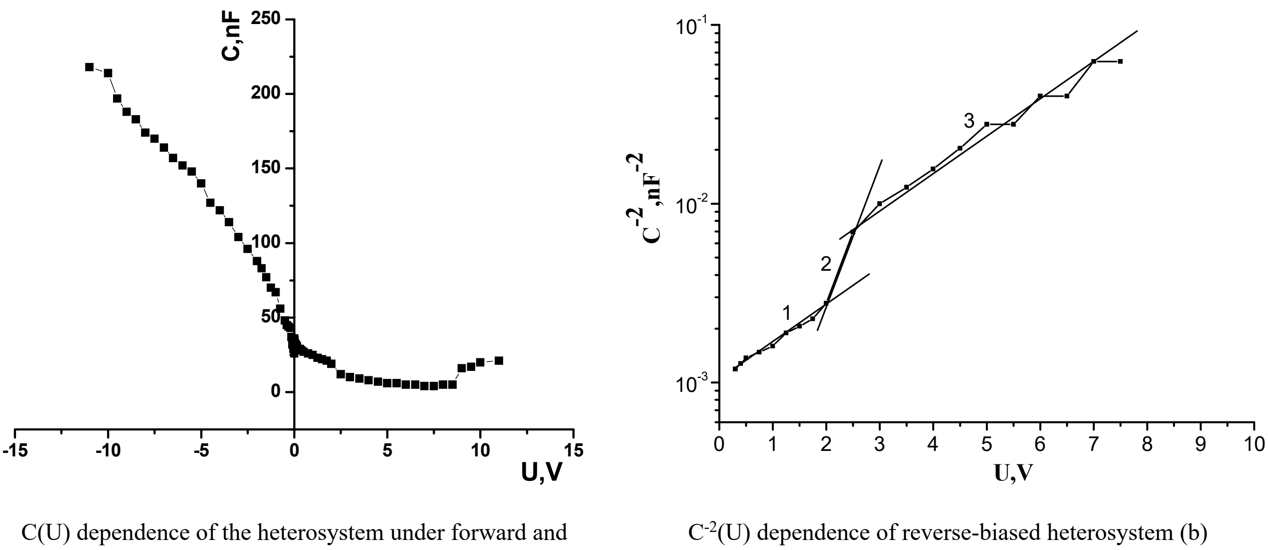
The first term of expression (6) describes the current resulting from thermal generation of charge carriers at a rate n_p/τ_n in a base layer of width L_n behind the space charge region, and the second part of formula (6) represents the current resulting from generation of charge carriers in the space charge region. Since the space charge region is depleted of carriers, $p_n \leq n^2_i$ and the Shockley-Read statistics [49] are written as r-g=-$n_i/2\tau_0$, i.e., under reverse bias, carrier generation in the space charge region predominates over recombination. In semiconductors with a large band gap, such as silicon, gallium arsenide, and cadmium telluride, n_i is small, and therefore the generation current clearly predominates.

In section (1) of the reverse I–V characteristic (Fig. 7), the current is indeed limited by the generation of carriers in the space charge layer, and the contribution to it of the current of the space charge region is insignificant. Further on the I–V characteristic, there is section (2), where the dependence of the current on the voltage has the form $I=AV^{\alpha}$, $\alpha=2.44$. Such a section of the I–V characteristic can take place in long diodes at low and high levels of injection of minority carriers. Consequently, electrical neutrality is ensured at each point in the base of such diodes. However, the studied diodes with a Schottky barrier are connected in the reverse direction, and the space charges in them are quite thick. Therefore, it is assumed that there is an injection of nonequilibrium electrons into the space charge layer. The injection of electrons into the space charge layer can occur from the interlayers of the grain boundary, as in [50], or from the rear contact made of Au, when a negative bias is applied to this contact. The appearance of the linear section of the current-voltage characteristic is because the thickness of the volume charge is filled with injected nonequilibrium electrons. As a result, the resistance of the entire part of the base is equalized. However, the concentration of nonequilibrium electrons injected from the rear contact (Au) is still less than the concentration of equilibrium carriers in the quasi-neutral part of the base layer of the structure.

After the section $I \sim V^{2.44}$ on the I-V characteristic (Fig. 7) there is a section $I \sim V^{5.55}$. With further increase in voltage, as can be seen from Fig. 7, a sharp increase in current is observed, and the exponent $\alpha \approx 5.55$. Such a section is called pre-breakdown. The section of sharp current growth appears with monopolar injection [51], when the sticking levels intersect with the Fermi quasi-level, or are at a very close distance. Electrons injected from the rear contact will affect the leakage currents and the noise characteristics of semiconductor devices.

One of the methods for obtaining information on the substantiated electrophysical parameters of semiconductors (the concentration of charge carriers and its distribution across the thickness of the sample; the concentration of impurities and defects; the density of surface states; the surface potential; the interface) is the frequency voltage-capacitance characteristic (VCC) method [52]. In the manufacture of electronic devices, the above-mentioned parameters of semiconductors are essential.

The capacitance-voltage characteristics of the structure under study show the presence of a metal-insulator-semiconductor structure (MIS structure) (Fig. 8).



C(U) dependence of the heterosystem under forward and reverse bias voltage (a)

C^{-2}(U) dependence of reverse-biased heterosystem (b)

Figure 8. Volt-capacitive characteristics of the CdS/Si/CdTe heterosystem at a frequency of f=50 kHz and t = 20°C

In the CdS/Si/CdTe heterosystem, the CdS layer is a high-resistance and compensated material, therefore this layer and the oxide layers formed during the deposition of CdS on the surface of the silicon wafer in vacuum behave as a dielectric, and the surface state densities N_{SS} in the heterojunction are slow surface states. The surface state density of the MIS structure is determined by the shift of the experimental VCC relative to the calculated curve at the same capacitance value [32]. It follows that $N_{ss}=\Delta VC/q$. The structure has a high surface state density at positive values of the surface potential, and the value of $N_{ss} \sim 9.2\times10^{10}$cm^{-2}.

When CdS type films are deposited on the silicon surface and manifest themselves as a high-resistance i-layer, it makes it possible to form transition i-layers of the CdS/Si and Si/CdTe interfaces on the boundary layer.

In Fig. 8.a it is seen how the thickness d_i=0.011 μm was determined from the capacitance C_i=217 nF using the formula for a flat capacitor $C=\varepsilon\varepsilon_0 S/d$. The thickness of the space charge W≈0.103 μm was determined from the minimum capacitance of the structure C_{min}≈23.3 nF. At thermodynamic equilibrium, its thickness, which was calculated from the capacitance of 31.7 nF in the absence of bias voltage, is equal to ~ 0.073 μm.

As is known, the thickness of the space charge narrows in the forward direction of the current. In the reverse direction, on the contrary, it expands with an increase in the bias voltage. From these experimental data, it also follows that the resistance of the space charge is the determining resistance of the entire structure, as evidenced by the coincidence of the value of its capacitance with the value of the dielectric capacitance in the C(U) characteristic.

The concentration of equilibrium electrons n_0 is determined by the capacity of flat bands and the steep section of the VCC characteristic (Fig. 8, b). To determine n_0 by the VCC characteristic, a steep section with two slopes is constructed in the $C^{-2}(U)$ coordinates: section 1 and section 2 (Fig. 8, b). According to the well-known formula (7) [51]:

$$n_0 = \frac{2}{q\varepsilon_0\varepsilon_S S^2}\frac{dV_D}{d(C^{-2})}, \tag{7}$$

The concentration of equilibrium electron carriers was determined. The concentrations of equilibrium electron carriers are $N_c \approx 3.3\times10^{15}$ cm^{-3} and $N_v \approx 4.1\times10^{14}$ cm^{-3}. By extrapolating the $C^{-2}(U)$ dependence onto the voltage axis U (Fig. 8, b) with the value of the structure capacitance C = 24 nF, V_D = (0.843 ± 0.02) eV was determined for n_0 in nSi. In addition, the value of the equilibrium electron concentration was estimated from the capacitance of flat bands [32]. The value of n_0 determined by VCC is consistent with the value of the equilibrium electron concentration of $3.6\cdot10^{12}$ cm^{-3} for nSi.

The effective concentration of charged acceptor centers is determined from the smoothly decreasing section of the volt-capacitance dependence $C^{-2}(U)$ of the heterostructure under study (Fig. 8, b), which has kinks and consists of three straight lines. This indicates the non-uniformity of the surface layer of the CdTe thin-base layer. The values of the lifetime τ_{01} and τ_{02} of nonequilibrium charge carriers are in agreement with the data given in the literature [36] for the lifetimes of carriers in CdTe with intrinsic conductivity.

The value of the lifetime of nonequilibrium carriers is determined by formula (8) [32]:

$$\tau_0 = \frac{n_i(2q\varepsilon\varepsilon_0)^{1/2}\,(V_2^{1/2}-V_1^{1/2})}{2N_{A,eff}^{1/2}\,(I_{r2}-I_{r1})} \tag{8}$$

and is $\tau_{01}\approx3.13\times10^{-7}$ s, $\tau_{02}\approx0.52\times10^{-7}$ s. The appearance of two values of τ_0 is due to two concentrations of charged local immobile centers. These centers were determined from the rapidly decreasing section of the dependence $C^{-2}(U)$, consisting of two straight lines 2 and 3 (Fig. 8, b), which indicates the inhomogeneity of the base layer of the CdTe film structure. The obtained results show that with an increase in the specific resistance of the base of the structure, the lifetime of equilibrium current carriers increases, therefore, the concentration of unfilled recombination centers decreases.

For the calculated C(U) characteristic, the concentration of equilibrium holes p_0 was determined by the capacitance of flat bands and by the steep section of the $C^{-2}(U)$ characteristic (Fig. 8, b), using the well-known formula (9) [53].

$$P_0 = \frac{2}{q\varepsilon_0\varepsilon_s S^2}\frac{dV}{d(C^{-2})} \tag{9}$$

and it is 8.3×10^{10} cm^{-3} and 2.6×10^{12} cm^{-3}. The capacity decreases with increasing reverse voltage (Fig. 8, b), which confirms the expansion of the space charge layer. This $C^{-2}(U)$ characteristic reaches a plateau at voltages of ~ 2÷2.5 V. This means that the space charge already at these voltages completely covers the entire thickness of the base (Si/CdTe) of the structure. When applying reverse bias to the thin-base CdS/Si heterojunction, the process of space charge expansion is compensated by the process of electron injection from the heterojunctions.

The experimental results confirm the formation of a CdS/Si heterojunction with a comparatively low density of surface states, despite the fact that the lattice constants of cadmium sulfide and silicon differ by more than 7%. The experimental results obtained become explainable if we take into account that an intermediate layer is formed in the heterojunction, which smooths out the difference in the lattice constants of cadmium sulfide and silicon [54]. Such intermediate layers can be solid solutions of these semiconductors or thin oxide layers that are present on the silicon surface during the formation of the CdS/Si heteropair.

Based on these data, a band diagram of the structure of (Au)CdS/Si/CdTe(Au) was constructed, shown in Fig. 9 (a complete description and calculated data of the band diagram of the structure are given in [28,31]).

The calculations of the electronic band structure performed are based on the density functional theory [29,55]. It is evident from the diagram that the reverse and forward currents at the interface of the CdS/Si and Si/CdTe heterojunction are limited by the resistance of the space charge layer. The space charge contains negatively charged mobile and immobile donor centers located at the interface between the layer and silicon due to the donor concentration in nSi, which is ten orders of magnitude greater than the carrier concentration in the chalcogenide layers. The isotypic CdS/Si junction has a contact potential difference with a value of $\Delta\varphi$=0.204 eV. Consequently, an enriched space charge layer appears at the interface of the CdS and Si junction, since the value of the metal work function $A_{(Au)}$=4.9 eV located in the CdS layer is less than the work function $A_{(Si)}$=5.01 eV.

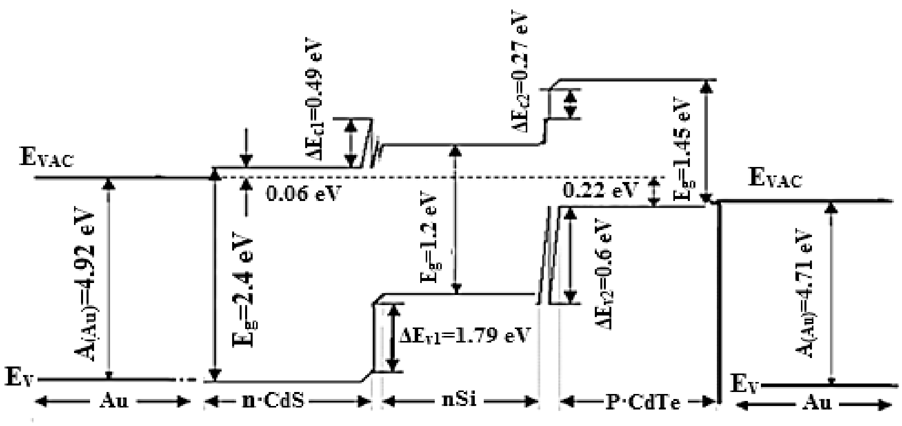


Figure 9. Energy band diagram of the heterosystem (Au)CdS/Si/CdTe(Au) [22,23]

From the band diagram of the structure (Au)CdS/Si/CdTe (Au) it is seen that the forward and reverse currents are limited by the resistance of the space charge layer at the interface of the heterojunction CdS/Si and Si/CdTe. This space charge consists of positively and negatively charged fixed donor (acceptor) centers, mobile holes and electrons, which are located in the surface layer of CdS and CdT. Since the concentration of electrons in nSi is ten orders of magnitude greater than the concentration of holes in the layer of CdS and CdT. Therefore, the external potential applied to the structure, including the contact potential difference, mainly falls on the space charge layer formed between Si and CdTe, and the surface states of Nss at the interface of the contacting semiconductors cadmium telluride and silicon can affect the height of the potential barrier, the nature of which is due to the difference in the constants of the crystal lattices of the heteropair and the technological conditions during the creation of heterojunctions [39,55-57]. The results of the VCC show that the structure under study behaves as an MIS structure and in it the main potential barrier is created in the near-surface layer of CdS at the interface of the CdS/Si heterojunction. These data also show that one of the reasons for the high concentration of nonequilibrium electrons in the high-resistance base (CdS) in the forward direction of the current is the relatively low density of surface states in the lower half of the silicon band gap, which is explained by the fact that in the forward direction of the current, nonequilibrium charge carriers interact with N_{ss} located in the lower half of the band gap, and in the reverse direction - with surface states located in the upper half of the silicon band gap.

CONCLUSIONS

Thus, the possibility of obtaining a heterosystem based on A^2B^6 compounds with potential barriers – (Au)CdS/Si/CdTe(Au) with a minimum density of surface states is shown, which is confirmed by measuring the height of the potential barrier, volt-capacitance methods. It is established that at current densities of $2.1\times10^{-7}\div0.35\times10^{-6}$ A/cm^{-2} in the studied CdS/Si/CdTe structure, the current is limited by recombination in the space charge layer. In this case, the difference of almost an order of magnitude between the calculated value of the lifetime of nonequilibrium carriers and its experimental value is explained by the participation of complex centers in the recombination processes, inside which the carriers are retained. Using the study of the current-voltage characteristics, it was determined that the CdS/Si/CdTe heterosystem has three sections at a constant temperature caused by the recombination process: a power-law section - $I\propto V^{2.44}$ (the effect of injection depletion), a sublinear section - $I\propto V^{0.78}$ (the recombination process), and a pre-breakdown section - $I\propto V^{5.55}$, which are explained by the fact that at low current densities the recombination of nonequilibrium carriers occurs through local centers, while complexes with internal electron exchange are responsible for recombination processes at high current densities. It was established that the CdS/Si heterojunction has a low density of surface states at the interface, which is evidenced by the high value of the rectification coefficient of the CdS/Si/CdTe structure and the appearance of a sublinear section in the reverse current-voltage characteristic in a wide range of bias voltages.

By studying the VC characteristics of the structure when turned on in the reverse direction, it was shown that after the complete coverage of the structure base by the space charge, electrons are injected from the rear contact, which determine the mechanism of charge transfer of the structure. In the compounds, Si is the source of electron injection. The results of VCC measurements of CdS/Si/CdTe heterostructures showed that the thickness of the space charge narrows in the forward bias, and in the reverse bias, it expands with increasing bias voltage. In addition, the resistance of the space charge is the determining resistance of the entire structure, since the CdS layer in the heterosystem is a high-resistance and strongly compensated material, which is evidenced by the fact that the structures belong to semiconductor MIS structures.

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МЕХАНІЗМ ПЕРЕНОСУ СТРУМУ В ТОНКОСНОВНІЙ ГЕТЕРОСИСТЕМІ НА ОСНОВІ СПОЛУК A^2B^6

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Представлено можливість створення гетеросистеми на основі сполук A^2B^6 з потенційними бар'єрами (Au)CdS/Si/CdTe(Au) з мінімальною густиною поверхневих станів, що підтверджено вимірюваннями висоти потенційного бар'єру на основі вольтажних методів. Визначено різні експоненціальні залежності струму від напруги при прямих зміщеннях, пов'язані зі зміною кінетичних параметрів бази структури CdS/Si/CdTe, і виявлено, що при густинах струму $2{,}1\times10^{-7} \div 0{,}35\times10^{-6}$ А/см$^{-2}$ у досліджуваній структурі CdS/Si/CdTe струм обмежується рекомбінацією в шарі просторового заряду. Показано, що при прикладенні до структури зворотного зміщення база структури повністю покривається просторовим зарядом, що супроводжується інжекцією електронів з тильного контакту, що, у свою чергу, визначає механізм передачі струму структури.
Ключові слова: *гетеросистема; осадження; база; шар; бар'єр; фотодіод; густина струму; ємність; SEM; зонна діаграма*