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EFFECT OF GATE OXIDE AND BACK OXIDE MATERIALS ON SELF-HEATING EFFECT IN FinFET

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The self-heating effect on the fin field effect transistor (FinFET) is investigated. The dependence of the lattice temperature in the channel center of the transistor on the thickness of the gate oxide, as well as the back oxide, is simulated. Different types of the most used oxide materials (SiO_2, HfO_2, and Si_3N_4) and their combination, SiO_2+Si_3N_4, are considered for gate and back oxides. 3D simulation is performed using Sentaurus TCAD. It is shown that the lattice temperature slowly and monotonically decreases with increasing gate oxide thickness. However, the lattice temperature is monotonically increasing with the thickness of the back oxide. This behavior of the lattice temperature depends on the relation between heat generation and dissipation rates in the transistor channel. A difference in the heat conductivity of the oxide materials explains the obtained behavior of the lattice temperature. Also, the lattice temperature dependence on the gate oxide thickness is explained by the increase in the contact area between the gate oxide and the gate with increasing gate oxide thickness. Besides this, it is accounted that the Joule heat generation rate depends on the drain current, which also depends on the oxide materials.
Keywords: *3D simulation; FinFET; Self-heating effect; Gate oxide; Back oxide*
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INTRODUCTION

One of the main tasks of nanoelectronics is to reduce power consumption and increase the degree of integration of integrated circuits (ICs). This task is connected with the considerable reduction in size of the transistors that make up the integrated circuit. Along with other elements, metal-oxide-semiconductor field-effect transistors (MOSFETs) are one of the most important components of ICs. The reduction in the size of MOSFETs leads to the appearance of various degradation effects, including short-channel effects (SCE), self-heating effect (SHE), Negative Bias Temperature Instability (NBTI), etc.

SCEs are strongly manifested in MOSFETs based on planar technology, which is one of the initial technologies for manufacturing MOSFETs. To increase the resistance of MOSFETs to short-channel effects, a structure of a vertical (or Fin) MOSFET (FinFET) was proposed instead of planar MOSFETs, with gate lengths of the order of 20 nm and lower, which operate in the inversion mode [1]. FinFET has three gates and, as a consequence, has a high degree of electrostatic integrity that ensures high immunity against short-channel effects [2].

One of the features of the FinFETs is that they are based on silicon-on-insulator technology. This feature is characterized by the fact that the channel of the transistor borders an oxide layer, the so-called back oxide layer (BOX). This feature leads to the manifestation of a self-heating effect in FinFET due to the low thermal conductivity of the oxide layer, leading to a low dissipation rate of heat generated in the channel of the transistor [3], [4], [5]. As a result, increasing the temperature in the transistor channel leads to changing the drain current and, as a consequence, degradation of the I-V characteristics of the FinFET.

Therefore, finding the oxide materials that increase the immunity of the transistors against SHE and that are compatible with FinFET fabrication technology is a very important task. In this work, the impact of the BOX materials, as well as gate oxide materials, on the temperature in the transistor channel is investigated [6], [7]. SiO_2, HfO_2, Si_3N_4, and combination SiO_2+Si_3N_4 are mainly used in FinFET fabrication technology, and therefore, in this research, these materials are considered as BOX as well as gate oxide materials.

TRANSISTOR STRUCTURE PARAMETERS AND SIMULATION MODELS

The cross-section along the channel of the 3D structure simulated in this work, a silicon-based FinFET, is shown in Fig. 1. The silicon-based transistor's channel is n-type. TiN is used as a gate material. Geometrical sizes of the different parts of the transistor and channel doping level are presented in Table 1. In the simulation, the gate oxide thickness varies between 1 and 1.5 nm, while the back oxide thickness varies between 10 and 1000 nm.

In the simulation, Sentaurus TCAD software is used. For the estimation of the self-heating effect, the drift-diffusion transport model in conjunction with the thermodynamic transport model was used. To account for quantum effects, the quantum correction Density gradient was also used. The doping-dependent mobility model and velocity saturation in the high field are taken into account. Coulomb and phonon scatterings are included in the simulation model to consider the

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mobility degradation at the interface as the high-k material HfO_2 is used as the gated oxide. A simulation drift-diffusion transport model was calibrated by comparing the I-V characteristics of the simulated transistor with experimental results presented in [8], [9], [10]. The results of the comparison given in Fig. 2 show a good agreement.

Table 1. Geometrical and physical parameters of the considered transistor

Parameter	Designation	Value
Source and drain doping level	N_d	5×10^{18} cm^{-3} (n-type)
Channel doping level	N_a	1×10^{16} cm^{-3} (p-type)
Gate oxide (HfO_2, Si_3N_4) thickness	t_{ox}	t_{EOT} = 1.0-1.5 nm
Channel thickness	T_{si}	9 nm
Channel width	W_b	22 nm
Back oxide layer (SiO_2, HfO_2, SiO_2+Si_3N_4) thickness	T_{box}	10-1000 nm
Gate length	L_{gate}	10 nm

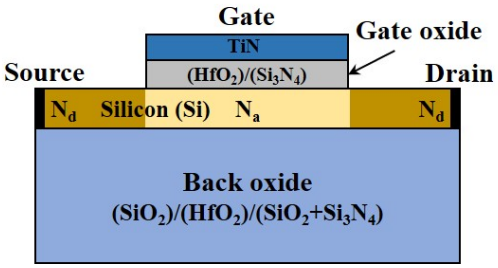

Figure 1. Simulated FinFET cross-section structure

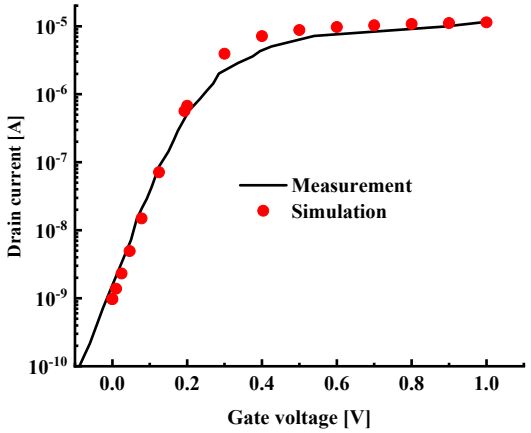

Figure 2. Comparing the I-V characteristics of the simulated and experimental transistors for L_{gate} = 25 nm and V_{ds} = 50 mV

SIMULATION RESULTS AND DISCUSSION

The dependence of the temperature in the channel center on the thickness of gate oxide in FinFET for HfO_2 and Si_3N_4 as gate oxide, and SiO_2, HfO_2, and SiO_2+Si_3N4 as back oxide is simulated. The results of the simulation are shown in Fig. 3. Results show, that the lattice temperature very slowly decreased with increasing the gate oxide thickness for all considered oxide materials, while the contact area between the gate oxide and the channel increased monotonically with increasing the gate oxide thickness (Fig. 4). Increasing the contact area lead to increasing heat dissipation rate, however drain current, and as consequence heat generation rate, practically is not changed with increasing the gate oxide thickness. Obviously, in this case, the heat generation rate has a greater effect than the heat dissipation rate.

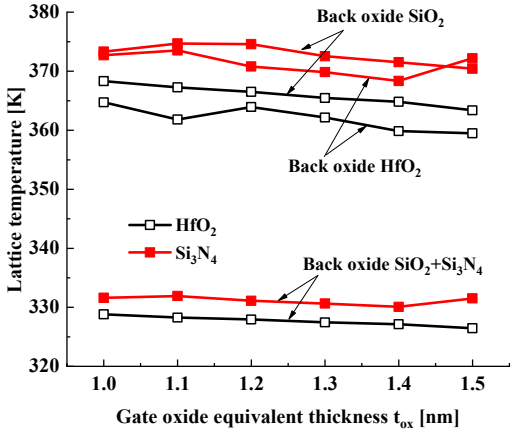

Figure 3. Dependence of the lattice temperature in the channel center on the gate oxide equivalent thickness for different gate oxide and back oxide materials.

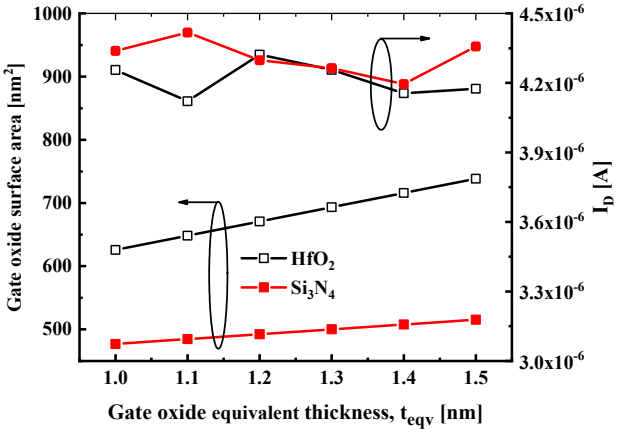

Figure 4. Contact area and drain current dependence on the gate oxide equivalent thickness. BOX is HfO_2

It is seen in Fig. 3 that in the case of using HfO_2 as gate oxide, the lattice temperature is lower than at using Si_3N_4, for all BOX materials. This dependence correlates with drain current dependence on the gate oxide thickness (Fig. 4).

The temperature dependence on the gate oxide thickness is the result of the combined effect of the dielectric constant, thermal conductivity, and the thickness of the gate oxide

Lattice temperature dependence on the BOX thickness T_{box} is monotonous, and the temperature grows with increasing BOX thickness for all considered BOX materials. This dependence is in agreement with [11], [12] and at higher thicknesses is expressed by the formula (1).

$$\Delta T = \frac{(P_t \cdot T_{box})}{K_b \cdot A}, \tag{4}$$

where P_t stands for the heat power generated by the current in the channel, K_b is the heat conductivity of the oxide layer, and A represents the area of the contact surface between the oxide layer and the channel.

Fig 5 shows the dependence of the lattice temperature in the FinFET channel center on the back oxide thickness (TBOX) for different oxide materials. It can be seen that the lattice temperature increases monotonically with increasing TBOX, regardless of the material type. This is explained by the fact that a thicker BOX layer increases the distance between the heat source (channel) and the heat sink (metal contact), thereby reducing the heat dissipation efficiency. Among the considered materials, the combination SiO_2+Si_3N_4 shows the lowest temperature values, which can be attributed to its highest thermal conductivity, as indicated in Table 2.

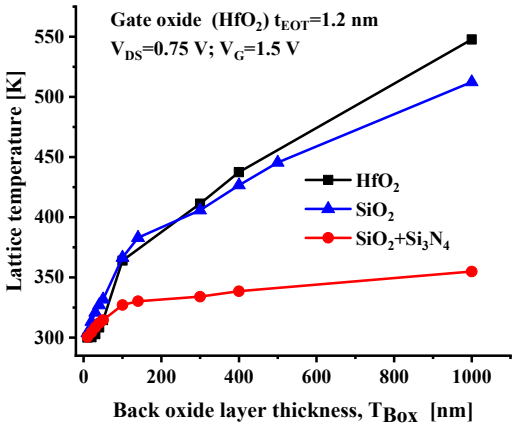

Figure 5. Lattice temperature dependence on the thickness of the BOX for different materials

Table 2. Thermal Conductivity of the oxide materials

Oxide Material	Thermal Conductivity K_b (W m^{-1} K^{-1})
HfO_2	2.3
SiO_2	1.4
Si_3N_4 (SiO_2+Si_3N_4)	18.5

CONCLUSION

Results of the simulation show that the lattice temperature in the center of the FinFET channel depends on the gate oxide as well as the back oxide material. More considerable dependence on the temperature of the materials is seen for back oxide, where the maximal difference in the temperatures lies in the range between 50 and 170 K for BOX thicknesses from 100 to 1000 nm. The maximal temperature difference in using different considered gate oxide materials is approximately 10K in all considered ranges of oxide thicknesses. The material of the oxide layers influences the drain current, but a substantial influence on the temperature is the thermal conductivity of the back oxide material.

The highest immunity against the self-heating effect is achieved using HfO_2 as gate oxide material and SiO_2+Si_3N_4 as back oxide material in the considered range of oxide materials in this work.

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ВПЛИВ МАТЕРІАЛІВ ОКСИДУ ЗАТВОРУ ТА ОКСИДУ ЗВОРОТНОГО ШАРУ НА ЕФЕКТ САМОРОЗІГРІВУ У FinFET

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Досліджено ефект саморозігріву польового транзистора з ребрами (FinFET). Моделюється залежність температури решітки в центрі каналу транзистора від товщини затворного оксиду, а також оксиду зворотного шару. Для затворних та зворотних оксидів розглядаються різні типи найбільш використовуваних оксидних матеріалів (SiO_2, HfO_2 та Si_3N_4) та їх комбінація SiO_2+Si_3N_4. 3D-моделювання виконано за допомогою Sentaurus TCAD. Показано, що температура решітки повільно та монотонно зменшується зі збільшенням товщини затворного оксиду. Однак, температура решітки монотонно зростає зі збільшенням товщини зворотного шару оксиду. Така поведінка температури решітки залежить від співвідношення між швидкістю тепловиділення та розсіювання в каналі транзистора. Отримана поведінка температури решітки пояснюється різницею в теплопровідності оксидних матеріалів. Також залежність температури решітки від товщини затворного оксиду пояснюється збільшенням площі контакту між затворним оксидом та затвором зі збільшенням товщини затворного оксиду. Крім того, враховується, що швидкість джоулевої тепловиділення залежить від струму стоку, який також залежить від оксидних матеріалів.

Ключові слова: *3D-моделювання; FinFET; ефект самонагріву; затворний оксид; зворотний оксид*