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IMPACT OF LOCAL OXIDE TRAPPED CHARGE ON ELECTRICAL AND CAPACITANCE CHARACTERISTICS OF SOI FINFET

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In this work, the influence of the local oxide trapped charge on the transfer $I_d - V_g$ characteristics and capacitance of the gate-to-source (drain) connection of the silicon-on-insulator (SOI) structure-based FinFET is simulated. $I_d - V_g$ characteristics are simulated by using the drift-diffusion transport model. Capacitance-Voltage characteristics of the gate-to-source capacitance are simulated by using a small AC signal method. The $I_d - V_g$ characteristics and gate-to-source (gate-drain) capacitance are investigated at different linear sizes and positions of the local oxide trapped charge along the channel. The results of the simulation show that the threshold voltage monotonically decreases with an increase in the linear size of the local charge, and gate-to-source capacitance monotonically increases with an increase in the distance between the source-channel border and the center of the local charge.

Keywords: *FinFET; Lokal charge; Gate-to-source capacitance; p-n junction; C-V dependence*

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1. INTRODUCTION

One of the main devices of nanoelectronics is field effect transistors, particularly Fin Field Effect Transistors (FinFET), which is continuously scaled over the last several decades. As a result of scaling, the characteristics of the transistors are being degraded due to short channel effects [1], [2], self-heating effect [3], [4], impact of oxide (interface) trapped charge [5], [6]. Among these degradation effects can be noted as appreciable the effects of hot carrier injection [7], [8], bias temperature instability [9]–[11], off-stress [12], and the impact of the radiation-induced charge [13]. These degradation effects are mainly connected with injection or/and generation charges in the oxide layer or at the oxide-semiconductor interface. In nanoscale FETs the random telegraph noise, induced by a single oxide (or interface) trapped charge, can also be considerable [14], [15]. The impact of these effects should be taken into account at designing and using analog as well as digital integrated circuits based on FETs.

The oxide trapped charge can affect MOSFET parameters such as threshold voltage and subthreshold slope of the transfer characteristics. Consequently, it leads to degradation of the transistor characteristics. Therefore, to determine the mechanisms and reasons of the charge trapping it is expediently develop the methods of estimation the position and distribution of the trapped charge along the channel.

Well-known methods for detecting the oxide and interface trapped charge in planar MOSFETs are methods connected with measuring current-voltage and capacitance-voltage dependencies [16]–[18]. Particularly, for this purpose, measurements of subthreshold drain current [16] and gate-to-substrate capacitance-voltage dependence [17], [18] are used. However, these methods should be modified in the case of SOI FinFET, because of specific features of the transistor's structure connected with the presence of the back oxide layer between channel and substrate. Therefore, it is important to consider and study the features of the impact of trapped charges on I-V and C-V dependences in SOI FinFET.

One of the simple and fast methods of diagnostics to detect the charge trapped in the oxide layer or at the interface is based on measurements of the capacitance-voltage characteristics of lateral source (drain)-channel p-n-junctions [19]. Experimental evidence of this method is presented in [13], [20], [21]. It is shown that the non-uniform distribution of the charge in the oxide layer or at the semiconductor-oxide interface is appropriately reflected in source-channel (drain-channel) p-n-junction capacitance [13], [19], [20], [22]. Thus, the distribution along the channel of the trapped charge should also be reflected in other capacitances connected with lateral source-channel (drain-channel) junctions.

In this work, dependencies of the drain current and threshold voltage on linear size and position of the oxide trapped charge, along the channel, are considered for SOI FinFET. The capacitance method mentioned above and first suggested for planar MOSFET [19] is modified for application in SOI FinFET. The modified method will be used to simulate the dependence of the gate-to-source capacitance, C_{gs}, on the position of the local oxide trapped charge.

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This paper is organized as follows. In Section 2, we present the description of the considered transistor parameters, simulation conditions, and approaches used. Simulation results with discussions are presented in Section 3. Finally, some concluding remarks are formulated in Section 4.

2. TRANSISTOR PARAMETERS, SIMULATION CONDITIONS, AND APPROACHES

The structure of the simulated SOI FinFET is shown in Figure 1. The geometry and parameters of the simulated FinFET are shown in Table 1.

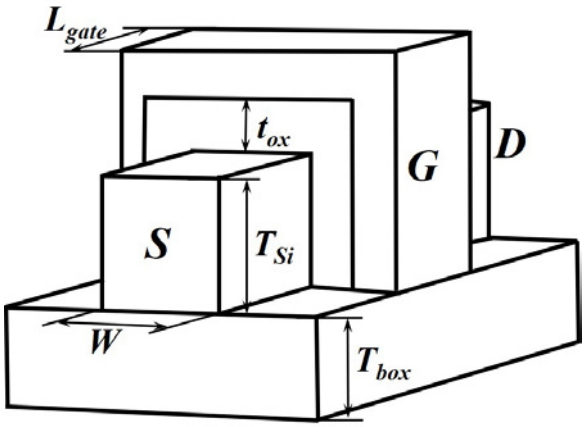


Figure 1. 3D structure of the simulated SOI FinFET

3D simulation were conducted using Advanced TCAD Sentaurus software. Transfer characteristics of the FinFET were simulated by using drift-diffusion as well as thermodynamic transport models to choose an adequate transport model. The results of the simulation are shown in Figure 2. It is shown in the figure that at gate voltages up to $V_g - 1V$, both $I_d - V_g$ curves are the same. And at higher gate voltages drain current is lower at using the thermodynamic transport model, which is connected with increasing the temperature in the channel. In simulation, the range of the gate voltages was limited to 1V; therefore, the use of the drift-diffusion and thermodynamic transport models is equivalent. We used a simple drift-diffusion transport model to save resources (power and time).

Table 1. Here is the caption of your table

Parameter	Designation	Value
Channel doping level (p-Si)	N_a	$1 \cdot 10^{15} cm^{-3}$ (n-type)
Source and drain doping level (n-Si)	N_d	$1 \cdot 10^{20} cm^{-3}$ (n-type)
Gate oxide (HfO_2) thickness	t_{ox}	2.5 nm
Channel thickness	T_{Si}	30 nm
Channel width	W	12 nm
Back oxide layer (SiO_2) thickness	T_{box}	100 nm
Gate length	L_{gate}	25 nm

Density gradient quantum corrections were used to account for quantum effects because transistor sizes are on the nanometer scale. In the mobility model, the doping dependence and velocity saturation at high fields were taken into account. The model used in the simulation was calibrated by comparing $I_d - V_g$ characteristics with experimental results presented in [23] (Figure 3). The experimental $I_d - V_g$ curve presented in [23] was normalised to the width of the channel; therefore, to compare with the simulation results, it was recalculated for the whole transistor width.

In this work, the dependencies of the drain current Id and threshold voltage Vth on the position, L, and width, D, along the channel of the local oxide trapped charge were considered. The dependence of the capacitance C_{gs} of the gate-to-source (drain) connection on the position L was also considered. At considering the dependence on the position L, the width of the local oxide trapped charge D is fixed and equal to 5 nm. At considering the dependence on the width, the local oxide trapped charge is located at the drain end of the gate oxide layer and expands to the center of the oxide layer (Figure 4). The homogeneously charged area models local oxide trapped charge in the oxide layer. Charge density in the charged area is $1 \cdot 10^{12} cm^{-2}$ (or $4 \cdot 10^{18} cm^{-3}$), and it corresponds to the value that can take place in MOSFETs [18].

The choice for consideration of the gate-to-source capacitance C_{gs} is based on the following. The main idea of the capacitance method suggested in [20] to detect the oxide (interface) trapped charge is connected with the impact of

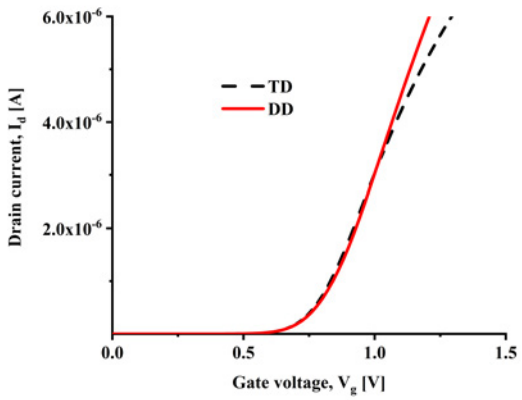


Figure 2. Transfer $I_d - V_g$ characteristics simulated using thermodynamic (TD) and drift-diffusion (DD) transport models.

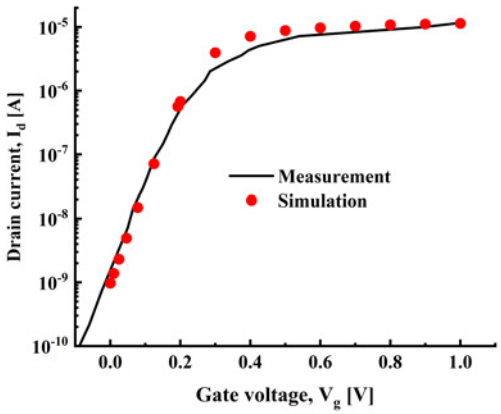


Figure 3. Calibration of the simulation model by comparing simulated and experimental [23] $I_d - V_g$ characteristics of the SOI FinFET transistors with L_{gate} = 25 nm and V_d = 50 mV.

the oxide or/and interface trapped charge on lateral source-channel (drain-channel) p-n-junction capacitance, C_{p-n}, in planar MOSFET. In the case of SOI FinFET, C_{p-n} capacitance can not be measured directly because of the presence BOX layer between the source and substrate. However, this capacitance is included in the capacitance of the gate-to-source (gate-to-drain) connection (Figure 5). Therefore, changes in C_{p-n} capacitance due to oxide trapped charge should be reflected in C_{gs} capacitance.

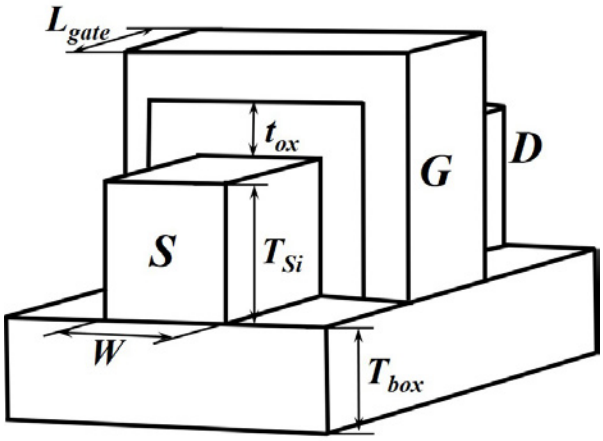


Figure 4. Cross-section of the FinFET showing local oxide trapped charge.

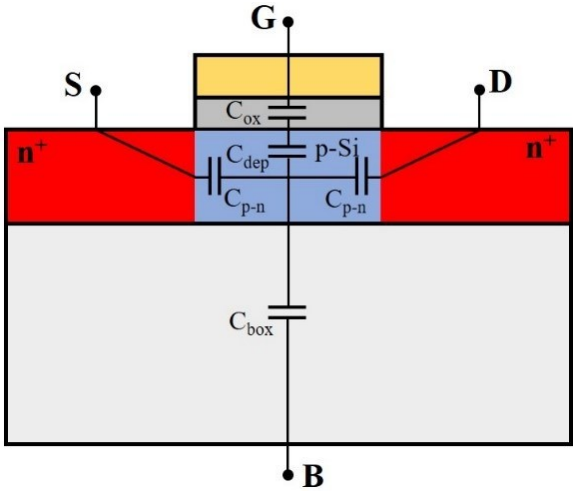


Figure 5. Cross-section of the simulated SOI FinFET with pictured capacitances between contacts.

The gate-to-source connection as well as the gate-to-drain connection contains the following capacitances connected in series: gate oxide capacitance Cox, oxide-semiconductor interface depletion layer capacitance, C_{dep}, source-to-channel p-n-junction capacitance, C_{p-n}. Only in depletion mode, the depletion layer capacitance, C_{dep}, significantly contributes to C_{gs} capacitance. However, in the considered case, a transistor is in accumulation mode, because in the simulation, the p-type source (drain) region is biased by the positive pole of the voltage source relative to the gate. Thus, establishing the accumulation mode at the semiconductor surface, near the oxide-semiconductor interface, results in dismissing the capacitance C_{dep}. Consequently, the resulting capacitance C_{gs} can be expressed by the following formula (1):

$$C_{gs} = \frac{C_{p-n} \cdot C_{ox}}{C_{p-n} + C_{ox}} \tag{1}$$

here, C_{ox} is gate oxide capacitance per unit area, which does not depend on the applied voltage. Estimations show, that C_{p-n} is significantly less than Cox because width of the depletion layer of the source-to-channel (drain-to-channel) p-n-junction is approximately 0.1 µm while gate oxide thickness t_{ox} = 2.5 nm. Thus, in accordance with the formula

(1) C_{gs} is determined mainly by C_{p-n}, which is very sensitive to the distribution of oxide trapped charge [13], [20]. Consequently, in this work, it is simulated the dependence of the C_{gs} on the position of the local oxide trapped charge along the channel.

C-V dependence of the gate-to-source (gate-to-drain) capacitance were simulated with using the small AC signal method. Signal with frequency 1 MHz is used in simulation. The capacitance C_{gs} is simulated at different position of the local oxide trapped charge along the channel.

The local charge with fixed width D=5 nm, in the oxide layer at a distance L from the source-channel border (Figure 4) impacts on the carrier distribution in the channel. Consequently, this impact should be reflected in the source-to-channel junction capacitance and hence in the C-V dependence of the gate-to-source capacitance.

FinFET has symmetry relative the channel center, hence the gate-to-source and gate-to-drain capacitances should be same. Therefore, in the following, mainly the gate-to-source capacitance is considered.

3. SIMULATION RESULTS AND DISCUSSIONS

3.1. Impact of the local charge on electrical characteristics

Figures 6 and 7 illustrate the simulation results regarding the dependence of drain current on the gate voltages at different positions and the width of the local oxide trapped charge. The figures demonstrate that the local oxide trapped charge considerable influence on the transfer $I_d - V_g$ curve, especially in the region above the threshold voltage.

Figure 6b presents the simulation results depicting the dependence of the drain current above threshold voltage on the position L of the local oxide trapped charge. The figure demonstrates that the dependence is nonmonotonic. The drain current is maximal at the position of the local charge near the channel center. However, the dependence of the drain current on the width D is monotonic with saturation at higher D (Figure 7b). The observed behaviors of the drain current can be attributed to the appropriate behavior of the threshold voltage (Figure 8).

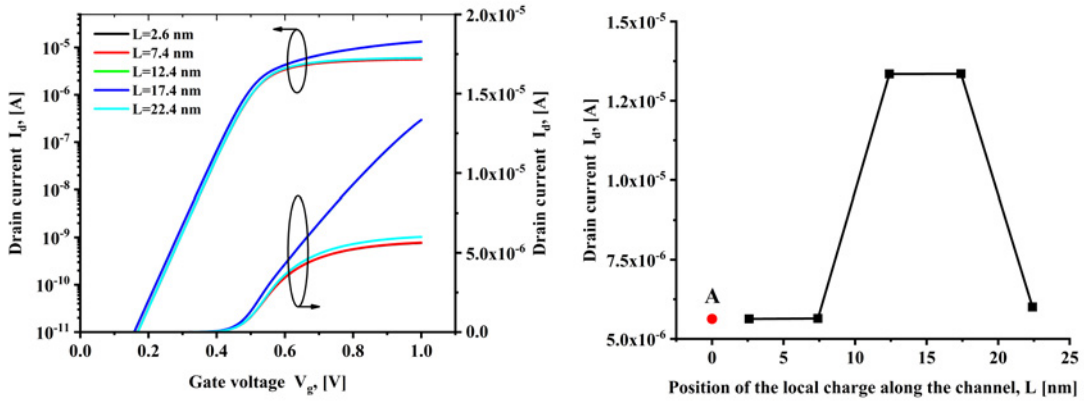
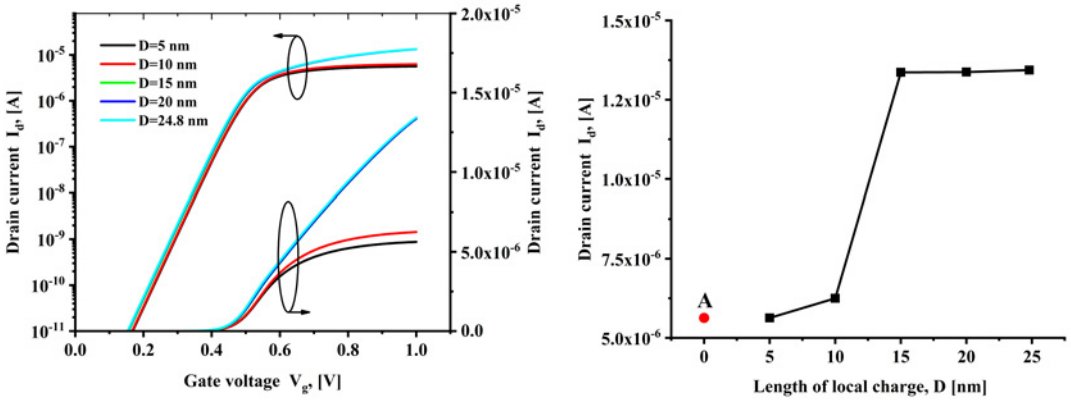


Figure 6. (a) $I_d - V_g$ characteristics at various position, L, of the local oxide trapped charge. (b) Dependence of the drain current, at V_g=1V, V_d=0.75V, on the position, L, of the local oxide trapped charge. Point A corresponds to the case of without oxide trapped charge.

The behavior of the drain current at the change of the position and linear size of the local oxide trapped charge is correlated with the behavior of the threshold voltage. A decrease in the threshold voltage leads to an increase in the drain current and vice versa; an increase in the threshold voltage leads to a decrease in the drain current. The observed changes of threshold voltage with change of the position and width of the local oxide trapped charge can be understood in terms of the change of the distribution of channel surface potential and the corresponding inversion layer carrier concentration along the channel, induced by the field of the local trapped charge.

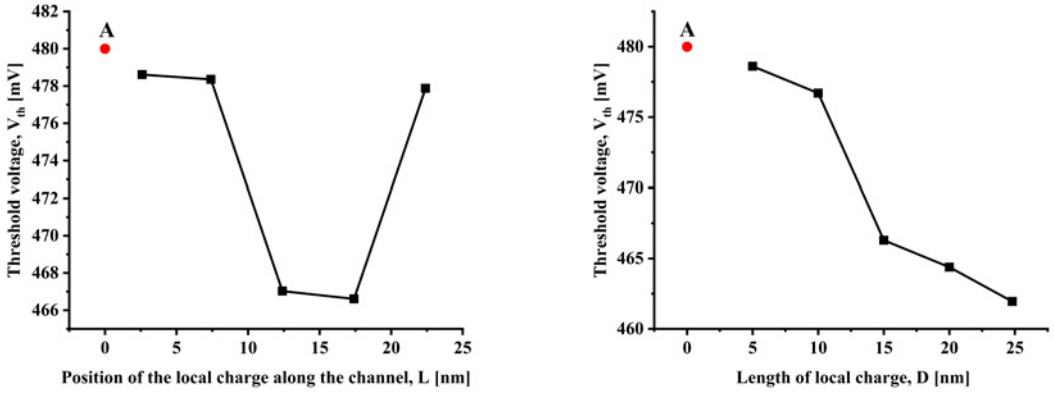
Originally, in case of absence, the local oxide trapped charge, potential distribution along the channel surface has a bell-shape with a maximum in the middle of the channel and with approximately zero value near the metallurgical border of the source-channel and drain-channel p-n junctions [25]–[27]. Hence, the maximal impact of the local oxide trapped charge on potential distribution and consequently on threshold voltage, can take place at the position of the local charge in the center of the channel. Figure 8a illustrates an appropriate relationship between threshold voltage and position of the local oxide trapped charge.

The threshold voltage shows a monotonic dependence on the linear size of the local charge, D (Figure 8b). This behavior of the threshold voltage is the same as the dependence of threshold voltage on the value of oxide trapped charge in planar long-channel MOSFET [15]. Hence, determining the shift of threshold voltage allows estimating the value of oxide



(a) **(b)**

Figure 7. (a) $I_d - V_g$ characteristics at various widths, D, of the local oxide trapped charge. (b) Dependence of the drain current, at V_g=1V, V_d=0.75V, on the width, D, of the local oxide trapped charge. Point A corresponds to the case of absence of the oxide trapped charge.



(a) **(b)**

Figure 8. Threshold voltage dependencies on the position, L, (a) and the width, D, (b) of the local oxide trapped charge. Point A corresponds to the case of absence of the oxide trapped charge.

trapped charge in SOI FinFET using the method suggested in [16]. In case of a change in the slope of the subthreshold I-V curve, it also should be accounted for in estimating the change in threshold voltage.

3.2. Impact of the local charge on gate-to-source (gate-to-drain) capacitance

Figure 9 illustrates the simulation results regarding the C-V dependence of the gate-to-source capacitance, C_{gs}, for different position, L, of the local oxide trapped charge. The figure demonstrate that the capacitance C_{gs}, at high applied voltages is significantly and monotonically depends on L (Figure 10). The position corresponding L=2.5 nm (point B in Figure 10) is an exception in this dependence. This is attributed to the fact that in this position the local charged area is in contact with the end of the oxide layer. Consequently, the edge effect is manifested, leading to a considerably high capacitance C_{gs},

The observed increase in the capacitance C_{gs} is linked to the impact of the local trapped charge on carrier concentration within the channel. Indeed, Figure 11 demonstrates that trapping of the charge in the oxide layer leads to an increase in the carrier concentration near the channel surface at all positions of the local charge. In accordance with the definition of capacitance, this results in higher capacitance C_{gs}. In fact, by definition, the capacitance is defined in accordance with formulas (2),

$$C_{gs} = \frac{dQ_V}{dV} \tag{2}$$

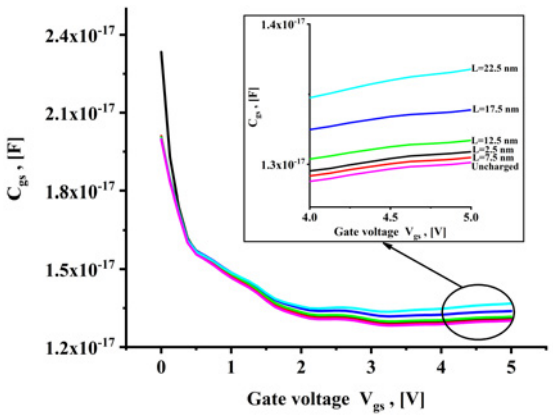


Figure 9. C-V dependence of gate-to-source capacitance C_{gs} at different positions of the local trapped charge.

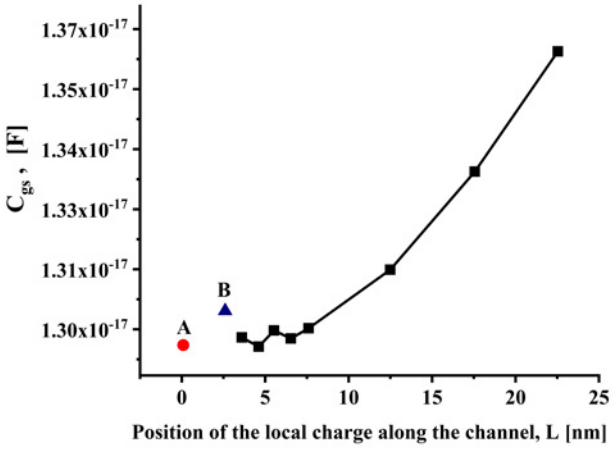


Figure 10. C_{gs} dependence on L at V_{gs}=4.5 V. Point A corresponds to C_{gs} when the local trapped charge is absent, point B corresponds to the position of the local trapped charge at the source end and is in contact with the oxide end (L=2.5 nm).

where dQ_V is a change of the charge in the capacitor C_{gs} at a change in the applied voltage by d_V. Trapping of the local charge into the gate oxide layer leads to adding a charge dQ_{LC} in capacitance C_{gs}, besides dQ_V Therefore, the formula (2) can be rewritten by the following expression (3)

$$C_{gs} = \frac{dQ_V + dQ_{LC}}{dV} \tag{3}$$

It follows from this expression that the capture of local charge leads to an increase in the capacitance C_{gs}

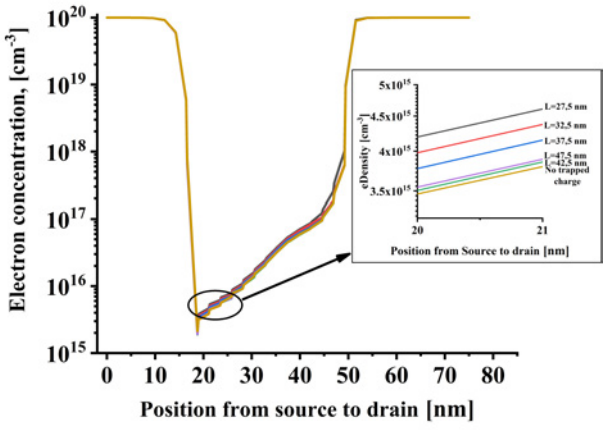


Figure 11. Distribution of electron density along the channel at depth 2nm from the channel surface, at different positions L of the local oxide trapped charge. V_{gs} = 4.5 V

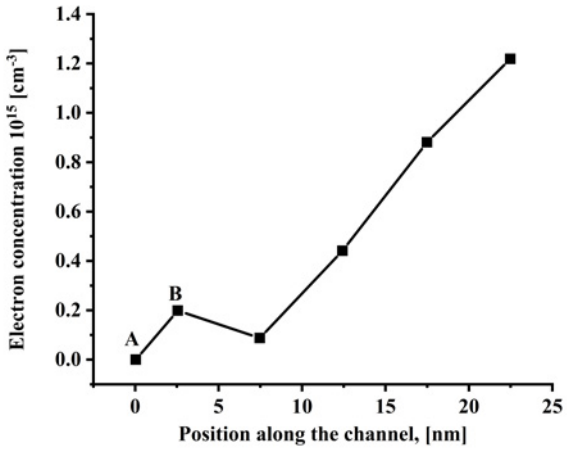


Figure 12. Dependence of the electron density in the channel at a depth of 2 nm from the surface on the position of the local oxide trapped charge. Point A corresponds to the case without oxide trapped charge, and point B corresponds to the position of local charge L=2.5 nm. V_{gs} = 4.5 V

The charges dQ_V and dQ_{LC} are caused by applied voltage and trapped charge, respectively, which are proportional to the change of carrier concentration in the channel. Figure 12 illustrate dependence of the electron density in the channel at a depth 2 nm from the surface on position of the local oxide trapped charge. This dependence correlate with dependence of C_{gs} on the position of local trapped charge shown in Figure 10.

The structure of FinFET has symmetry relative vertical axis passing through the channel center, therefore dependence of gate-to-drain capacitance, C_{gd}, on position L should be the same as the dependence of C_{gs} on position L, but with reversed character. It means that C_{gd} should decrease with increasing L. Indeed, such a character of the dependence is seen in the dependence of C_{gd} on L, carried out from simulation (Figure 13). The relationship between C_{gs} and C_{gd} dependences on the L can be used to estimate the position of the local trapped charge along the channel. For this purpose, the dependence of the ratio C_{gs}/C_{gd} on L can be used (Figure 14).

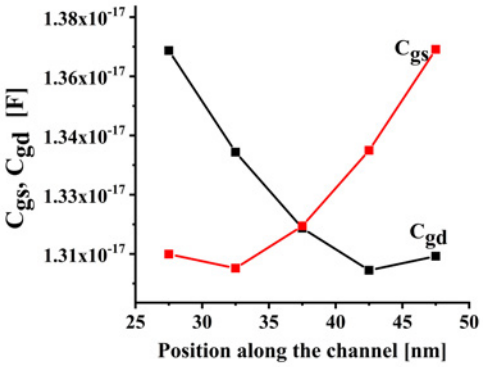


Figure 13. Dependence of C_{gs} and C_{gd} on the position of the local oxide trapped charge, L, along the channel.

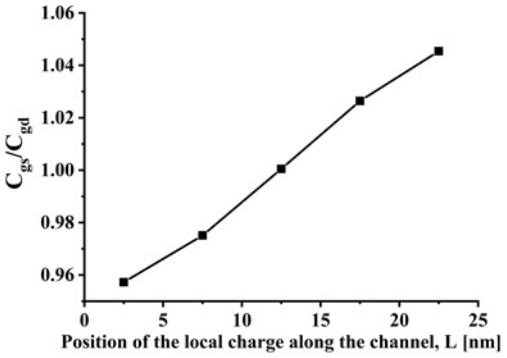


Figure 14. Dependence of the ratio C_{gs}/C_{gd} on the position of the local oxide trapped charge, L, along the channel.

Figure 14 demonstrates that in the case of trapping the local charge at the source side relative to the channel center, the ratio C_{gd}/C_{gs} is less than 1. Value of the ratio C_{gd}/C_{gs} is more than 1 in case of localisation the trapped charge at drain side relative the channel center. In case of localization the trapped charge in the center between source and drain end, the value of the ratio C_{gd}/C_{gs} is equal to 1.

4. CONCLUSIONS

Simulation results show, that the threshold voltage monotonically depends on the linear size, D, along the channel of the charge trapped at drain end of the oxide layer. It allows to estimate integral value of trapped charge in oxide layer in the SOI FinFET as well as in planar MOSFET.

At high applied voltages, gate-to-source capacitance, C_{gs}, monotonically depends on the position of the local oxide trapped charge along channel. C_{gs} monotonically increase with increase distance between source and center of the local charge. Such dependence is explained by the influence of the local charge on the carrier distribution at the surface of the channel. The position of the local charge at the end of the oxide layer is an exception in the mentioned above dependence due to edge effect.

It is shown that the ratio C_{gd}/C_{gs} depends linearly on the position of the local oxide trapped charge along the channel in SOI FinFET. This dependence allows to develop a method to detect the charge in oxide layer and to estimate the distribution of the oxide trapped charge along the channel.

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ВПЛИВ ЛОКАЛЬНОГО ЗАРЯДУ, ЗАХОПЛЕНОГО В ОКСИДІ, НА ЕЛЕКТРИЧНІ ТА ЄМНІСНІ ХАРАКТЕРИСТИКИ SOI FinFET

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У цій роботі моделюється вплив локального заряду, захопленого в оксиді, на передавальні характеристики Id-Vg та ємність між затвором і витоком (стоком) транзистора FinFET на основі структури кремнію на ізоляторі (SOI). Характеристики Id-Vg моделюються з використанням моделі дрейф-дифузійного переносу. Ємнісно-напругові характеристики затвор-виток моделюються за допомогою методу малого змінного сигналу (AC). Досліджено залежність характеристик Id-Vg та ємності затвор-виток (затвор-сток) від різних лінійних розмірів і положень локального заряду в оксиді вздовж каналу. Результати моделювання показують, що порогова напруга монотонно зменшується зі збільшенням лінійного розміру локального заряду, а ємність затвор-виток монотонно зростає зі збільшенням відстані між межою виток-канал і центром локального заряду.

Ключові слова: *FinFET; локальний заряд; ємність затвор-виток; p-n перехід; C-V залежність*