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MODELING AND THEORETICAL STUDY OF p-n HETEROJUNCTIONS BASED ON CdTe/Si: BAND ALIGNMENT, CARRIER TRANSPORT, AND TEMPERATURE-DEPENDENT ELECTROPHYSICAL PROPERTIES

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This paper presents a comprehensive theoretical study of p-n heterojunctions formed between cadmium telluride (CdTe) and silicon (Si) over the temperature range of 0 K to 800 K. We focus on band alignment, carrier transport mechanisms, and the temperature-dependent electrophysical properties of the heterojunctions. Through modeling approaches, we explore the energy band structure, intrinsic concentration, intrinsic electrical conductivity, and the impact of temperature variations on the heterojunction characteristics. Our findings provide insights into optimizing the performance of CdTe/Si heterojunctions for applications in photovoltaics and optoelectronics.
Keywords: *Modeling; Built-in potential; Heterojunction; Band gap; Intrinsic concentration; Intrinsic electrical conductivity*
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1. INTRODUCTION

Heterojunctions have garnered significant attention in recent decades due to their extensive applications in optoelectronic and photovoltaic devices. Among these, CdTe/Si heterojunctions stand out for their potential to enhance the performance of solar cells and photodetectors, attributable to the advantageous combination of their respective material properties [1]. Cadmium Telluride (CdTe), a II-VI compound semiconductor, is renowned for its suitability in photovoltaic (PV) solar cell production, primarily owing to its exceptional absorption coefficient ($\alpha > 10^4$ cm^{-1}) and ideal band gap of 1.5 eV [2, 3]. Silicon (Si), with its established manufacturing processes, is widely utilized in the electronics industry. The integration of these two materials into p-n heterojunctions can leverage the inherent benefits of each, resulting in improved device performance and expanded functionality [4, 5].

The formation of a p-n junction between CdTe and Si introduces complexities related to band alignment and carrier transport. The band alignment of heterojunctions plays a critical role in charge separation and recombination processes, which are pivotal for device efficiency. Numerous models have been proposed to investigate the electronic properties of these heterojunctions, particularly emphasizing band offsets, energy level alignments, and carrier mobility. Despite the promising potential of CdTe/Si heterojunctions, the temperature-dependent behavior remains a significant challenge, necessitating further theoretical and experimental exploration [5-7]. Notably, doping within CdTe-based heterojunctions profoundly influences their electrical characteristics. For instance, the introduction of lead (Pb) into CdTe films has been observed to diminish hole concentration by over three orders of magnitude due to self-compensation effects, while also resulting in a decrease in charge carrier mobility with increasing temperature during annealing [8]. To achieve an efficient photoelectric heterojunction, it is imperative to investigate the electronic properties of the semiconductors involved, considering the effects of doping impurities and their optimal spatial distribution within the heterojunction [9, 10]. These insights are vital for elucidating carrier transport mechanisms and band alignment in CdTe/Si heterojunctions, particularly under varying temperature conditions.

Temperature fluctuations can significantly affect carrier transport mechanisms by altering the band gap, carrier concentration, and mobility within the materials. Specifically, the band gap of CdTe decreases with increasing temperature, which leads to variations in conduction and valence band offsets at the heterojunction interface. Such changes critically impact the overall performance of the heterojunction, especially in applications such as thermophotovoltaics and high-temperature sensors [11,12]. Furthermore, studies focusing on temperature dependence are essential for understanding the heterojunction's resilience to operational stresses, particularly in environments characterized by fluctuating thermal conditions.

Previous investigations have sought to model these effects through both analytical and numerical approaches. Workshops on mathematical modeling of semiconductor heterostructures have delved into the numerical aspects of carrier transport across various temperature regimes [13-17]. Additionally, experimental studies have assessed the structural and electrical properties of CdTe/Si heterojunctions [7,18-25]. Nevertheless, significant gaps persist in the theoretical understanding of temperature-dependent band alignment and carrier dynamics, especially when contextualized within real-world operational scenarios.

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A thorough understanding of band alignment and charge carrier transport in CdTe/Si heterojunctions is crucial for optimizing device performance. This paper endeavors to provide an in-depth theoretical exploration of the band structure, carrier dynamics, and temperature-dependent properties of CdTe/Si heterojunctions.

Additionally, various experimental methods for fabricating p-n junction structures utilizing CdTe material have been extensively researched. Emerging fabrication techniques for CdTe/Si heterojunction structures include vapor-liquid-solid (VLS) [26] growth, transient laser-induced grating (TLIG), close-spaced vapor transport (CSVT) technique [29], chemical vapor deposition (CVD) [28], transmission electron microscopy (TEM) [21] and metalorganic vapour-phase epitaxy MOVPE [17]. These methodologies have enabled researchers to successfully create innovative structures such as nanowire arrays and nanocones, which are specifically designed to enhance light absorption in CdTe/Si heterojunction structures.

This study aims to model and analyze the band alignment and carrier transport mechanisms in CdTe/Si heterojunctions, with a particular emphasis on their temperature-dependent electrophysical properties. Employing advanced simulation tools such as TCAD Sentaurus and MATLAB [4,5], we will investigate how temperature influences the key parameters that dictate the efficiency of these heterojunctions. Moreover, we will compare theoretical results with experimental data to furnish a comprehensive understanding of the factors that enhance or impede the performance of CdTe/Si-based devices.

2. MATERIALS AND METHOD

As previously mentioned, the Band Gap emerges as the most crucial parameter in semiconductor materials. Therefore, equation (1) enables the calculation of the varying temperature of the bandgap for Si, and CdTe. The formula for calculating the temperature dependence of the bandgap in semiconductor materials is typically described by the Varshni equation. It's expressed as:

$$E_g(T) = E_g(0) - \frac{\alpha \cdot T^2}{T + \beta} \tag{1}$$

Where $E_g(T)$ and $E_g(0)$ are bandgap at T and 0 K respectively, α and β are material-specific constants. This equation shows how the bandgap energy varies with temperature. The parameters α and β are experimentally determined constants for a particular semiconductor material [29]. The results of our new model and the corresponding equation (1) are depicted in Figure 3.

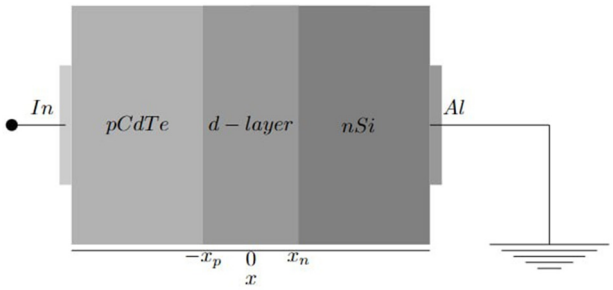

Figure 1. Schematic two-dimensional section of the p-n heterojunction structure based on pCdTe/nSi

The Figure 1 shows the 2D cross-sectional surface of the selected pCdTe/nSi sample. In this case, the p-type ohm contact is connected to In, and the n-type ohm contact is connected to Al. The band diagram corresponding to this heterojunction is shown in Figure 2.

The intrinsic concentration serves as a fundamental electrophysical parameter of semiconductor materials. The intrinsic carrier concentration n_i in a semiconductor is given by the equation:

$$n_i(T) = \sqrt{N_C(T) \cdot N_V(T)} \cdot \exp\left(-\frac{E_g(T)}{2kT}\right) \tag{2}$$

Where: $N_C(T)$ and $N_V(T)$ are the effective density of states in the conduction band and the effective density of states in the valence band. $E_g(T)$ is the energy bandgap, k is the Boltzmann constant and T is the absolute temperature.

The values of $N_C(T)$ and $N_V(T)$ depend on the material and are often expressed as functions of temperature [30,31]. The results of the corresponding equation (2) are depicted in Figure 4. Another electrophysical parameter influenced by temperature is internal conductivity. For the materials we have chosen, expression (3) corresponds to the equation for electrical conductivity as a function of temperature:

$$\sigma(T) = \sigma_0(T) \cdot \exp\left(-\frac{E_g(T)}{2kT}\right) \tag{3}$$

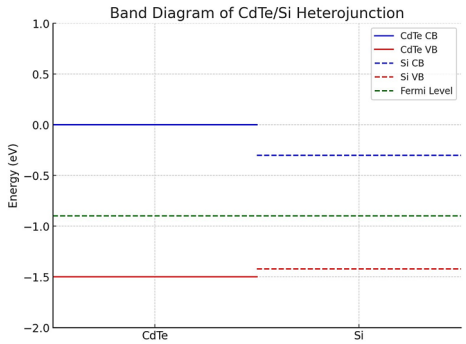

Figure 2. Band diagram of the pCdTe/nSi heterojunction

$\sigma(T)$ is the conductivity, $\sigma_0(T)$ is determined by expression (4), which indicates a linear dependence on temperature, and we have also considered that this expression is temperature-dependent. This expression (5) was analyzed in two cases: Case A, where $\sigma_0(T)$ is assumed to have a strong linear dependence on temperature, and Case B, where $\sigma_0(T)$ is considered temperature-independent. The difference between Cases A and B is presented and analyzed in Figure 5.

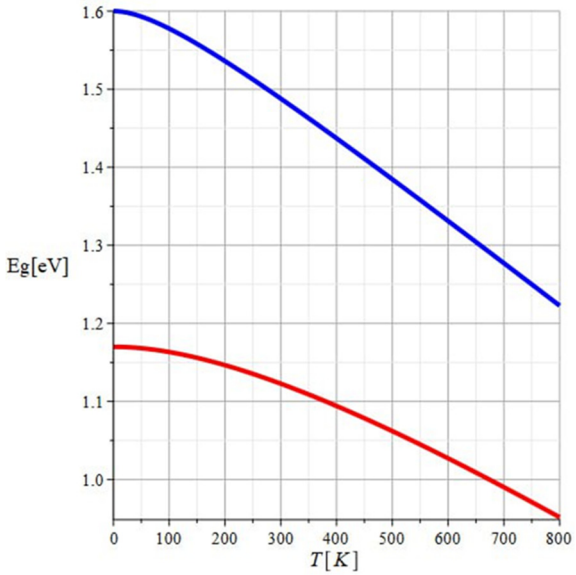

Figure 3. Band gap of a semiconductor as a function of temperature: red line for Si, blue line for CdTe

$$\sigma_0(T) = q \cdot (n(T) \cdot \mu_n(T) + p(T) \cdot \mu_p(T)) \,. \tag{4}$$

Here, $n(T)$ and $p(T)$ are the electron and holes concentration, $\mu_n(T)$ and $\mu_p(T)$ are the electrons and hole mobility which represents the temperature dependence. If we consider equal intrinsic electrons and holes concentration $n_i(T) = p_i(T)$, expression (3) can be substituted with expression (5).

$$\sigma_i(T) = \sigma_{0i}(T) \cdot \exp\left(-\frac{E_g(T)}{2kT}\right) \tag{5}$$

The graphical representation of the result from expression (5) is depicted in Figure 5, illustrating intrinsic electrical conductivity as a function of temperature. The obtained results were derived by considering the temperature dependence of the electrophysical parameters in our model.

3 RESULTS AND DISCUSSION

This graph illustrates the well-known phenomenon of band gap narrowing with increasing temperature in semiconductor materials, which is crucial for understanding their electronic and optical properties across different operating temperatures.

Based on the analysis of Figure 3, we can conclude that both CdTe and Si exhibit significant temperature-dependent band gap narrowing from 200K to 800K. The CdTe band gap decreases more rapidly than Si, indicating a

stronger temperature dependence. This behavior has important implications for the performance of CdTe/Si heterojunction diodes across different operating temperatures.

Figure 4 shows at 300 K, $n_i(T) = 1.5 \cdot 10^{10} [cm^{-3}]$ for Si and $n_i(T) = 2 \cdot 10^{6} [cm^{-3}]$ for CdTe indicate the intrinsic carrier concentration. Figure 4 shows the inverse relationship of internal concentration to temperature in logarithmic form. The slopes of the lines for Si and CdTe differ, reflecting the intrinsic band gap differences between the two materials. Silicon, with a smaller band gap, shows a higher intrinsic carrier concentration at equivalent temperatures compared to CdTe, which has a larger band gap. The steeper slope of the CdTe line indicates that its intrinsic carrier concentration decreases more rapidly with decreasing temperature compared to silicon, highlighting its greater thermal stability at lower temperatures.

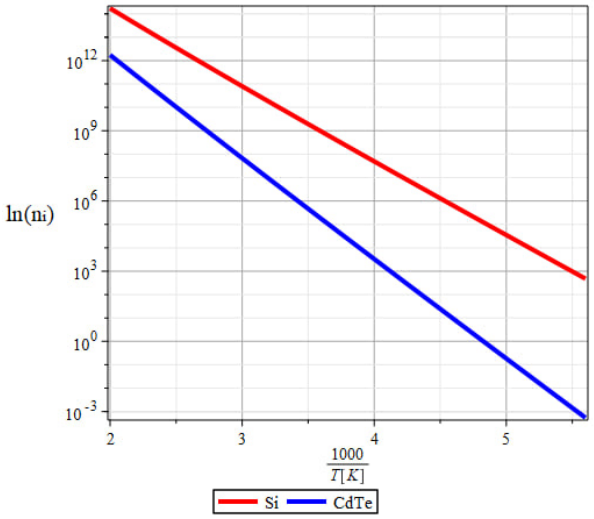

Figure 4. Internal electrical concentration as a function of temperature: red line for Si, blue line for CdTe.

At higher temperatures (left side of the graph), the intrinsic carrier concentration $n_i(T)$ of silicon is significantly higher than that of CdTe. This difference becomes more pronounced as the temperature increases due to silicon's smaller band gap, which allows for greater thermal excitation of carriers. At lower temperatures (right side of the graph), the intrinsic carrier concentration for both materials approaches lower values, but CdTe maintains a significantly lower ni compared to silicon. This makes CdTe advantageous for applications that require low carrier concentrations and minimal thermal noise at lower operating temperatures, such as infrared detectors and photovoltaics. The lower intrinsic carrier concentration in CdTe at elevated temperatures, compared to silicon, is advantageous for high-temperature applications where minimizing carrier generation is crucial, such as in high-performance photovoltaic cells. Conversely, the higher ni of silicon may benefit devices that rely on higher carrier densities for conduction, but it may also lead to increased leakage currents and thermal noise, potentially limiting its use in certain high-temperature or low-noise applications. The plot effectively illustrates the intrinsic properties of Si and CdTe and their suitability for different semiconductor applications. The analysis reveals that the choice of material for device fabrication must consider these temperature-dependent properties, especially in environments where thermal management is critical. The differences in band gap energies, as reflected in the slopes of the lines, underline the importance of material selection for optimizing the performance of semiconductor devices in varying temperature regimes.

Figure 5 shows the inverse relationship of conductivity to temperature in logarithmic form. The slope of the Si line is less steep compared to that of CdTe, indicating that silicon has a lower activation energy for conduction relative to CdTe. This suggests that at equivalent temperatures, silicon requires less energy to activate charge carriers, resulting in higher conductivity compared to CdTe. For CdTe, the steeper slope indicates a higher activation energy, which corresponds to its wider band gap. This translates to lower intrinsic conductivity at a given temperature, making CdTe more suitable for applications that require minimized leakage currents and stable performance at elevated temperatures. At higher temperatures (left side of the graph), both Si and CdTe exhibit higher conductivities, which is consistent with intrinsic conduction, where thermal energy is sufficient to excite electrons from the valence band to the conduction band. However, the higher intrinsic conductivity of Si highlights its lower band gap, enabling more electrons to be thermally excited. As the temperature decreases (right side of the graph), conductivity for both materials diminishes significantly, indicating reduced carrier availability and a shift toward extrinsic conduction dominated by impurity levels. This shift underscores the importance of doping strategies to maintain conductivity in these materials at low temperatures. CdTe's lower conductivity at higher temperatures, as evidenced by its steeper slope, suggests its advantage for applications in environments where maintaining low intrinsic carrier densities and minimal thermal noise is critical, such as in radiation detectors and high-temperature electronics. Silicon's higher intrinsic conductivity across a broad temperature range is advantageous for devices that operate efficiently at room temperature, such as microelectronics and photovoltaics. However, this characteristic may limit its effectiveness in high-temperature

environments where thermal noise must be minimized. The slopes of the linear regions for both materials can be used to extract the activation energies for conduction. This quantitative analysis provides a deeper understanding of the electronic properties of each material and helps optimize them for specific temperature-dependent applications. The Figure 5 effectively illustrates the contrasting thermal behaviors of Si and CdTe in terms of electrical conductivity. The observed differences highlight the significance of band gap energies and intrinsic material properties in determining their suitability for different semiconductor applications. The higher activation energy of CdTe suggests its preference for high-temperature environments where stability is key, while silicon's lower activation energy and higher conductivity make it ideal for room-temperature and low-temperature applications. These insights are crucial for developing efficient semiconductor devices tailored for specific operating conditions.

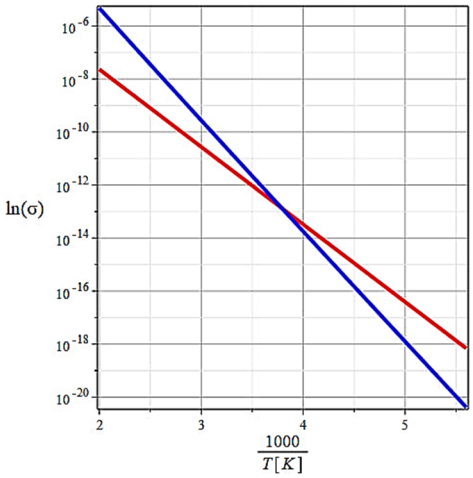

Figure 5. Internal electrical conductivity as a function of temperature: red line for Si, blue line for CdTe

CONCLUSIONS

In this study, we conducted a comprehensive modeling and theoretical analysis of p-n heterojunctions based on CdTe/Si, focusing on band alignment, carrier transport, and temperature-dependent electrophysical properties. The results indicate that the band gap and intrinsic carrier concentration of CdTe and Si are significantly affected by temperature variations. Specifically, the band gap of CdTe was found to decrease more rapidly with increasing temperature compared to Si, which highlights the strong temperature dependence of CdTe. This property is advantageous for high-temperature applications where thermal stability is critical. The intrinsic carrier concentration analysis revealed that silicon, due to its smaller band gap, maintains a higher carrier concentration at equivalent temperatures, making it suitable for applications requiring higher carrier densities.

The intrinsic conductivity analysis showed a linear relationship between conductivity and temperature. Silicon displayed a lower activation energy for conduction compared to CdTe, resulting in higher conductivity at room temperature. However, CdTe's lower intrinsic conductivity at elevated temperatures offers advantages for applications where minimizing leakage currents and maintaining stable performance are crucial.

These insights underline the importance of considering temperature-dependent properties when optimizing CdTe/Si-based devices for specific applications, such as photovoltaics, infrared detectors, and high-temperature electronics. Future work should focus on experimental validation of these theoretical findings and explore the influence of different doping strategies and material modifications on the performance of CdTe/Si heterojunctions under varying temperature conditions.

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REFERENCES

[1] R.A. Ismail, K.I. Hassan, et al., Mat. Sci. Sem. Processing, **10**, 1 (2007). https://doi.org/10.1016/j.mssp.2006.12.001
[2] M.H. Ehsan, H.R. Dizaji, and M.H. Mirhaj, Digest Journal of Nanomaterials and Biostructures, 7, 629 (2012).
[3] W.A. Pinheiro, V.D. Falcão, L.R. de Oliveira Cruz, and C.L. Ferreira, Materials Research, **91**, 47 (2006). https://doi.org/10.1590/S1516-14392006000100010
[4] J.Sh. Abdullayev, and I.B. Sapaev, Eur. J. Phys. **3**(49), 21 (2024). https://doi.org/10.31489/2024No3/21-28
[5] J.Sh. Abdullayev, and I.B. Sapaev, East Eur. J. Phys. (3, (2024). https://doi.org/10.26565/2312-4334-2024-3-39
[6] A. Cao, T. Tan, *et. al*., **545**, 323 (2018). https://doi.org/10.1016/j.physb.2018.06.035
[7] T.L. Chu, S.S. Chu, and S.T. Ang, J. Appl. Phys. **64**, 1233 (1988). https://doi.org/10.1063/1.341840
[8] Sh.B. Utamuratova, *et. al*., East Eur. J. Phys. (3), 385 (2023). https://doi.org/10.26565/2312-4334-2023-3-41
[9] V.I. Chepurnov, *et. al*., Computational Nanotechnology, **8**(3), 59 (2021). https://doi.org/10.33693/2313-223X-2021-8-3-59-68

[10] F. Bouzid, E. Kayahan, M.A. Saeed, *et al*., Applied Physics A, **130**, 222 (2024). https://doi.org/10.1007/s00339-024-07377-y
[11] C.H. Su, J. Appl. Phys. **103**, 084903 (2008), https://doi.org/10.1063/1.2899087
[12] M.N. Harif, *et. al*., Crystals, **13**(5), 848 (2023). https://doi.org/10.3390/cryst13050848
[13] S.H. Zyoud, *et. al*., Crystals, **11**, 1454 (2021). https://doi.org/10.20944/preprints202110.0346.v1
[14] *Mathematics for Semiconductor Heterostructures, Modeling, Analysis, and Numerics, International Workshop,* (2012). www.wias-berlin.de/workshops/msh2012
[15] E.A.B. Cole, *Mathematical and Numerical Modelling of Heterostructure Semiconductor Devices: From Theory to Programming*, (Springer-Verlag, London, 2009). https://doi.org/10.1007/978-1-84882-937-4
[16] M.V. Dolgopolov, *et al*., Samara U., Nat. Sci. Series, **30,** 64 (2024). http://dx.doi.org/10.18287/2541-7525-2024-30-1-64-81 (in Russian)
[17] J. Chavez, X. Zhou, S. Almeida, R. Aguirre, *et al*., J. Mat. Sci. Research, **5**(3), 1(2016). https://doi.org/10.5539/jmsr.v5n3p1
[18] B.S. Chaudhari, M. Niraula, *et. al*., J. Electronic Materials, **52**, 3431–3435 (2023). https://doi.org/10.1007/s11664-023-10318-9
[19] M.A. Razooqia, *et. al*., Ad. Mat. Research, **702**, 236 (2013). https://doi.org/10.4028/www.scientific.net/AMR.702.236
[20] X. Li, J. Lu, *et. al*., Nuclear Science and Techniques, **31**, 18 (2020). https://doi.org/10.1007/s41365-020-0723-y
[21] S.R. Bera, and S. Saha, Appl. Nanosci. **6**, 1037 (2016). https://doi.org/10.1007/s13204-015-0516-5
[22] E. Napchan, "HETEROJUNCTIONS OF CdTe ON Si", Imperial College of Science and Technology, (1987)
[23] D.J. Smith, *et al*., Materials Science and Engineering B, **77**, 93 (2000). https://doi.org/10.1016/S0921-5107(00)00480-3
[24] W.F. Mohammad, Circuits and Systems, **3**, (2012). http://doi.org/10.4236/cs.2012.31007
[25] V. Mizeikis, K. Jarašiunas, *et. al*., J. Crystal Growth, **214/215**, (2000). http://doi.org/10.1016/s0022-0248(00)00075-0
[26] M.C. Putnam, *et al*., Energy & Environmental Science, **3**(8), 1037 (2010). https://doi.org/10.1039/C0EE00014K
[27] A.V. Sukach, V.V. Tetyorkin, and N.M. Krolevec, Semiconductor Physics, Quantum Electronics & Optoelectronics, **2,** 13 (2010). http://journal-spqeo.org.ua/n2_2010/v13n2-2010-p221-225.pdf
[28] S. Osono, Y. Uchiyama, *et. al*., Thin Solid Films, **430,** 165 (2003). https://doi.org/10.1016/S0040-6090(03)00100-7
[29] I.B. Sapaev, *et. al*., E3S Web of Conferences, **410**, 02057 (2023). https://doi.org/10.1051/e3sconf/202341002057
[30] I.B. Sapaev, *et. al*., E3S Web of Conferences, **413,** 04009 (2023). https://doi.org/10.1051/e3sconf/202341304009
[31] I.B. Sapaev, *et. al*., E3S Web of Conferences, **413,** 04008 (2023). https://doi.org/10.1051/e3sconf/202341304008

МОДЕЛЮВАННЯ ТА ТЕОРЕТИЧНЕ ДОСЛІДЖЕННЯ p-n ГЕТЕРОПЕРЕХОДІВ НА ОСНОВІ CdTe/Si: ВИРІВНЮВАННЯ ЗОНИ, ТРАНСПОРТ НОСІЇВ ТА ЕЛЕКТРОФІЗИЧНІ ВЛАСТИВОСТІ, ЗАЛЕЖНІ ВІД ТЕМПЕРАТУРИ

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У цій статті представлено всебічне теоретичне дослідження p-n гетеропереходів, утворених між телуридом кадмію (CdTe) і кремнієм (Si) у діапазоні температур від 0 K до 800 K. Ми зосереджуємося на вирівнюванні зон, механізмах транспорту носіїв і температурно-залежних електрофізичних властивостях гетеропереходів. За допомогою підходів моделювання ми досліджуємо енергетичну зонну структуру, власну концентрацію, власну електропровідність та вплив зміни температури на характеристики гетеропереходу. Наші результати надають нові знання для оптимізації продуктивності гетеропереходів CdTe/Si для застосувань у фотоелектричних і оптоелектронних пристроях.

Ключові слова: *моделювання; вбудований потенціал; гетероперехід; ширина забороненої зони; власна концентрація власна електропровідність*