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SILICON *p-i-n* MESA-PHOTODIODE TECHNOLOGY

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The paper proposes the technology of silicon *p-i-n* mesa-photodiodes, which allows to exclude one high-temperature operation from the technological route. Reducing the number of thermal operations reduces the degree of degradation of the electro-physical characteristics of silicon during heat treatment, which also contributes to reducing the density of surface states at the $SiSiO_2$ interface. It is proposed to etch the mesa-profile by the method of chemical-dynamic polishing using a gold masking coating. The obtained photodiodes are cheaper than serial samples made by diffusion-planar technology and have higher sensitivity.

Keywords: *Silicon; Photodiode; Point Defects, Dislocations, Dark Current, Sensitivity*
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Semiconductor photodetectors are widely used in the development of automatic regulation and control systems for technological processes, research of the Earth's natural resources, in aircraft astronavigation systems, as well as in military equipment and cinema and photographic equipment [1]. The most widely used type of photodetectors is *p-i-n* photodiodes (PD) [2,3], and the main material of these products in the microelectronics industry is silicon due to its high manufacturability and widespread [4, 5].

The main parameters of PDs are responsivity, which determine the ability to register photosignals a certain range of wavelengths [6]. The main factor that ensures the maximum value of the photodiode photoresponsivity is the use of a base material with the highest possible values of the lifetime of minor charge carriers (τ) and resistivity (ρ), since these electrophysical characteristics determine the size of the region in which photogeneration of charge carriers occurs [7]. However, it should be noted that these parameters of silicon can degrade during high-temperature treatments [8, 9], so it is worth using technological methods and routes with a minimum number of thermal operations and with the lowest possible temperatures [10, 11].

The classical serial route of manufacturing *p-i-n* PDs based on *p*-Si using two-stage phosphorus diffusion from planar sources includes 4 thermal operations: oxidation, phosphorus predeposition, phosphorus driving-in and diffusion of boron [12]. It should be noted that two of these operations are high-temperature (T=1423 K), during which the degradation of electrophysical parameters occurs due to the diffusion of uncontrolled metal impurities with high diffusion coefficients or thermal shocks [13].

It is possible to exclude high-temperature expansion of phosphorus by using a single-stage diffusion of phosphorus from liquid diffusers PCl_3 or $POCl_3$, but in [14] we found that diffusion of phosphorus from liquid phased sources provokes the formation of a high density of structural defects (including dislocations), which in turn significantly reduces the percentage of usable products. This is due to the diffusion of phosphorus not only into the lattice nodes but also into the interstices, where the high density of electrically inactive impurities generates significant mechanical stresses compared to diffusion from planar sources, where alloying occurs along the lattice nodes.

Another method to reduce the number of thermal operations is to produce PDs with a mesa profile [15]. In this case, the first thermal operation is phosphorus diffusion, and the responsive elements (RE) are formed by etching mesa-structure, where the formed mesa-profile grooves are the gaps between the active elements of the photodiode crystal. In this case, there is no need for the first high-temperature oxidation. The problem of the described technique is the need to find a masking coating that allows masking the active regions of the photodiode from the effects of an aggressive etchant during etching. In [16], we conducted an experimental search for masking coatings and found that the use of AZ4533 [17] photoresist allows for a short time of etching in an $HNO_3 : HF : CH_3COOH = 9:2:4$ -compound etchant. The disadvantages of this photoresist are its high density, which causes problems during deposition, its high market price, and the inability to form a mesa profile of increased depth. We also proposed the use of a masking oxide deposited by RF cathodic sputtering for etching the mesa structure, since the etching speed of silicon oxide is significantly lower than that of silicon in the used etching agent. However, the application of the oxide film by this method provoked the formation of a high density of mismatch dislocations and, accordingly, the degradation of photodiode parameters, so this method proved to be ineffective [16].

Photodiodes with mesastructure have proven to be very promising products, so the search for the perfect technology and structure of these photodetectors is an urgent scientific and technical task. We have conducted a study on the use of a Au-masking coating for etching silicon in aggressive etchers. Accordingly, the purpose of this article is to investigate the

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possibility of manufacturing mesa-photodiodes using a Au- masking coating for etching, to study the parameters of these photodiodes and to compare them with the parameters of serial photodiodes manufactured using the classical diffusion-planar technology.

EXPERIMENTAL

The research was carried out in the manufacture of silicon 4Q *p-i-n* PDs with guard ring (GR) for operation at wavelength $\lambda_{op} = 1.064$ μm. PDs were made on the basis of single-crystal *p*-type silicon with resistivity $\rho \approx 18\text{-}22$ kΩ·cm and [111] orientation. The serial commercial samples were made by diffusion-planar technology according to the technological regimes given in [12] (PD$_C$). The thickness of the crystals reached 500-510 μm.

The crystals of the experimental mesa-photodiodes (PD$_M$) were produced by the following sequence of technological operations: phosphorus predeposition from solid-state planar phosphorus sources in a nitrogen atmosphere; phosphorus driving-in in a dry oxygen atmosphere; boron diffusion to the back side of the substrate; photolithography to create contact windows in the anti-reflective oxide; deposition of an Au-layer with an adhesive Chr-layer on the front side of the wafer; photolithography to open windows corresponding to the gaps between the REs (Fig. 1a) with the back side protected by a chemically resistant varnish; etching of the mesa-profile by chemical-dynamic polishing (Fig. 1b) according to the method described in [15]; photolithography to form Au-contact pads; application of Au with an adhesive chromium layer on the back side of the plate; and separation of crystals by cutting with a diamond cutting disc.


a b

Figure 1. Images of silicon wafers at different stages of PD manufacturing: after photolithography to open windows corresponding to the gaps between the REs; b) after chemical-dynamic polishing and photolithography to form Au-contact pads.

The depth of the mesa-profile should be greater than the depth of the diffuse phosphorus layer; in the case studied, the profile depth reached about 10 μm.

It is worth noting that the use of a "thin" gold film for prolonged etching in hydrofluoric acid or a polishing etchant can provoke the formation of etchings on the surface of REs due to the penetration of the etchant through the pores in the masking layer (Fig. 2). To ensure a proper masking effect, we used a gold thickness of 500-600 μm. The image of the final product is shown in Fig. 3.

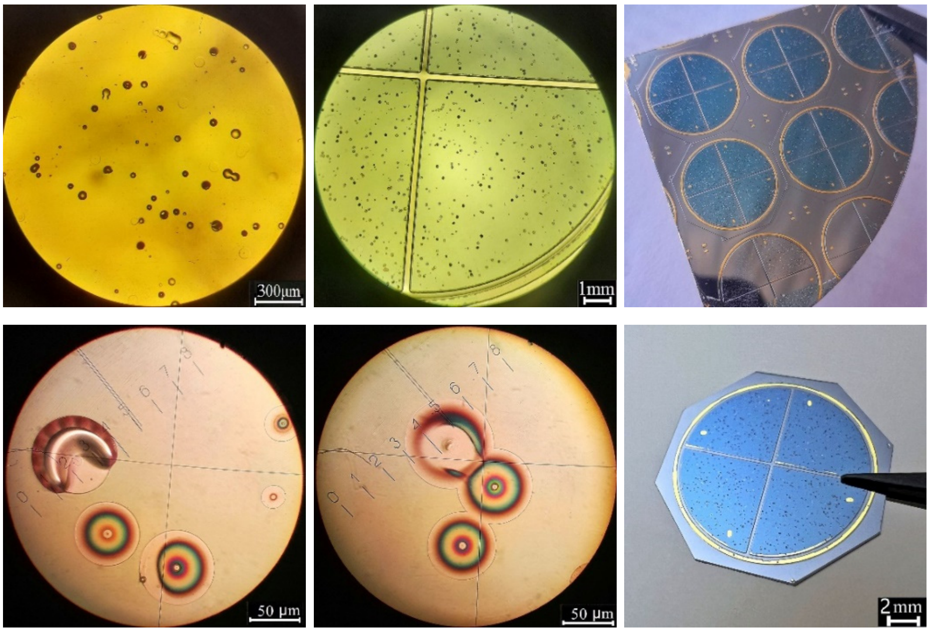
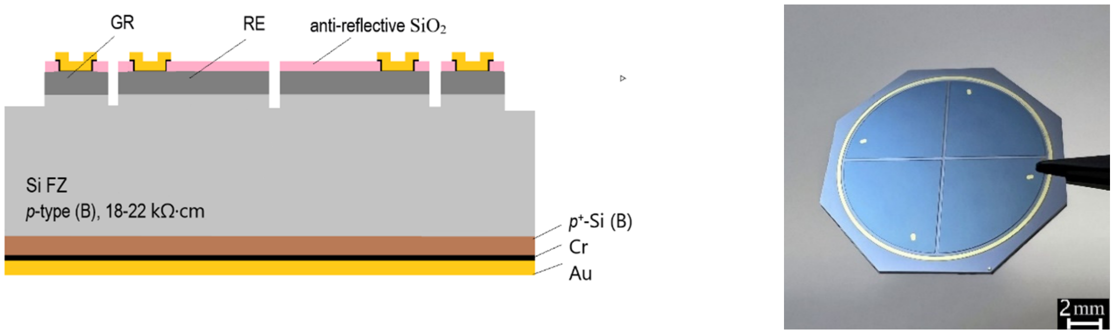


Figure 2. Images of photodiode crystals with etchings formed during oxide etching or chemical-dynamic polishing



a) b)

Figure 3. The image of the final *p-i-n* meza PD: a) cross-cection; b) final crystal.

The reverse *I–V* characteristics of PDs were measured using a hardware-software complex implemented on the basis of the Arduino platform, an Agilent 34410A digital multimeter and a Siglent SPD3303X programmable power source, which were controlled by a personal computer using software created by the authors in the LabView environment.

Determination of R_{con} was carried out according to the method shown in [18].

Monitoring of current monochromatic pulse responsivity was carried out by method of comparing responsivity of the investigated PD with a reference photodiode certified by the respective metrological service of the company. Measurements were performed when illuminating the PD with a radiation flux of a power of not over $1\cdot10^{-3}$ W; load resistance across the responsive element R_l= 10 kΩ,

RESULTS OF THE RESEARCH AND THEIR DISCUSSION

The reverse *I-V* characteristics of the PDs show that the experimental samples PD_M had slightly higher dark current values in the seventh reverse voltage range (Fig. 4). The reason for the difference in the dark current values is a slight increase in the area of the responsive elements and the release of the space charge region on the wafer surface due to the presence of the etching wedge and mesa profile [16]. These factors increase the value of the dark current due to the presence of a large number of surface states on the plate surface: a violation of the periodicity of the lattice potential of the crystal due to its break at the surface (Tamm levels) [17]; the presence of uncompensated valence bonds in surface atoms (Shockley levels) [18]; and the distortion of the lattice potential on the surface caused by adsorbed atoms and surface defects. The Tamm and Shockley levels characterize an ideal surface. On a real surface, however, surface levels caused by surface defects play a decisive role. These include point defects, which are atomic disturbances at individual points in the lattice (e.g., vacancies in lattice nodes or interstitial atoms), as well as linear and bulk defects (dislocations, pores, inclusions of another phase, etc.).

From the point of view of the band structure of a semiconductor, the presence of surface defects or adsorbed atoms leads to the formation of allowed levels in the band gap of the semiconductor, localized on the surface. Electrons from the valence band can move to these levels, and vice versa, electrons from surface levels can move to the conduction band, resulting in the semiconductor surface becoming charged, i.e. the formation of a semiconductor surface layer charged inversely to the volume of the so-called inversion layer.

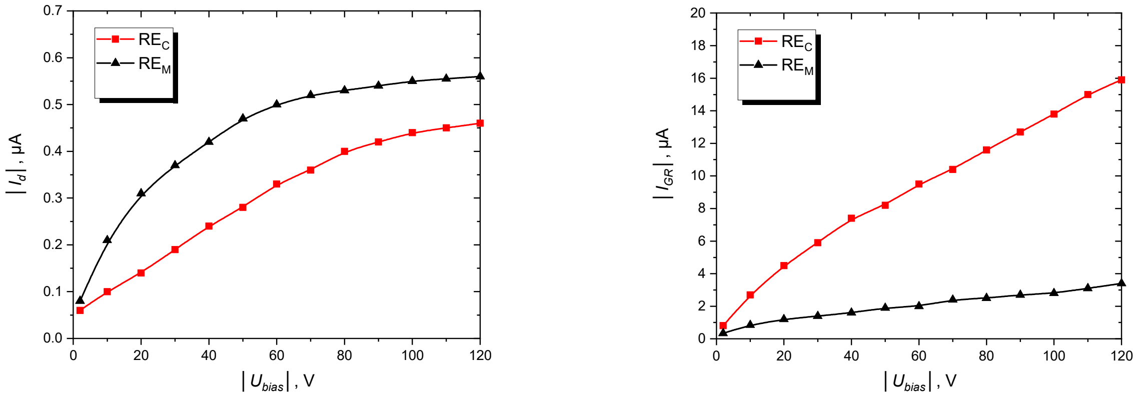
Accordingly, the growth of the dark current occurs due to the growth of the surface generation component (I_d^{surf}), which is directly proportional to the density of surface states (1)[14].

$$I_d^{surf.} = \frac{eN_{ss}v_{drift}\sigma_{ss}A_{p-n}}{2} \tag{1}$$

where σ_{ss} is capture cross-sectional area; N_{ss} – density of surface states; A_{p-n} - is the area that contributes to the surface component of the dark current; v_{drift} – is the average relative (relative to the center of re-combination) velocity of thermal charge carriers.

It should be noted that the mesa-profile formation was one of the last technological operations of the photodiode crystal manufacturing, after which no high-temperature operations were performed, so the etched surface can be considered quasi-perfect. An informative method for determining the presence of surface states is to measure the insulation resistance between responsive elements, as well as to measure the reverse dark *I-V*-characteristic of the guard ring, since the presence of surface states at the periphery of the crystal is crucial for the dark current of the guard ring, which contribute to the decrease in the surface component of the dark current when the area of space charge region of the guard ring is extended to the periphery.

In the experimental samples PD_M, the insulation resistance of all responsive elements and the GR was about $\sum R_{con}$≈3-5 MΩ, and in the serial samples PD_C produced by a single technological cycle, it was $\sum R_{con}$≈0.5-1 MΩ. Also, from the *I-V*-characteristics of the GRs, it can be concluded that the number of surface states in the mesa-photodiode is much lower, since this PD had a much lower value of the dark current of the guard ring (Fig. 4). The reason for the increase in the number of surface states is the presence of a larger number of high-temperature operations, in particular thermal oxidation, during which a large number of structural point defects are formed on the silicon surface, in particular the inclusion of interstitial silicon atoms or their accumulation due to oxygen diffusion [13], as well as a high probability of diffusion of uncontrolled impurities, in particular metals, due to their presence in the quartz tooling or improper chemical treatment of the wafers.



a) b)

Figure. 4. Reverse dark *I–V* characteristics of REs (a) and GRs (b).

It is worth noting that in [16] the depth of the mesa profile reached values only 1 μm greater than the depth of the diffusion layer of phosphorus. In this case, the difference in the values of the dark current of serial and mesa-photodiodes was minimal (up to 20 A). And in the case studied in this article, the depth of the mesa profile is twice as large as the depth of the diffusion layer, where a difference in the dark current values of ≥100 A was observed. Accordingly, it can be concluded that the dark current depends on the depth of the mesa profile, which correlates well with the above dependence of the dark current on the number of surface states captured by the spatial charge region.

It should be noted that the absence of the first thermal oxidation before phosphorus diffusion also allows us to obtain samples with a much lower dislocation density. It is known [13] that during the diffusion of phosphorus in the oxidizing atmosphere, local generation of defects, such as stacking faults and dislocations, occurs in places of localized disturbances of the wafer surface. And given the fact that the wafers before thermal operations undergo chemical and dynamic polishing, which minimizes the presence of surface defects, point defects formed during oxidation are the main centers of localization of dislocations. Accordingly, the absence of dislocation generation centers helps to reduce the probability of their formation.

Also, from the dependence of photodiode responsivity (Fig. 5) on voltage, it can be seen that mesa-photodiodes had a slightly higher photosensitivity than serial ones. This can be explained by a smaller number of generation and recombination centers and "traps" in the high-resistance region of the photodiode, where scattering and recombination of photogenerated charge carriers is possible, since, again, the absence of high-temperature oxidation reduces the probability of these "traps".

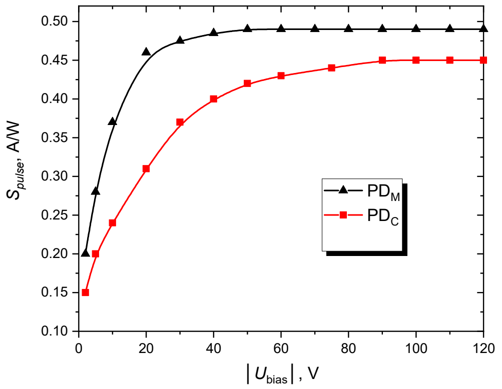


Figure 5. Dependence of the responsivity of PDs on the reverse bias voltage

It should be noted that the responsivity curve for the mesa-photodiode reaches saturation at lower values of the reverse voltages. This can be explained by the higher resistivity and lifetime of minority charge carriers, the degree of degradation of which is lower in PD$_M$ than in serial ones, since the sensitivity of the photodiode reaches a maximum when the space charge region (SCR) is extended to the entire thickness of the high-resistance region of the PD (or when the SCR and diffusion length of minor charge carriers are extended).

In addition to the obvious reduction in the cost of the proposed PDs, their advantage is the absence of the need to control the *C-V* characteristics of products after each thermal operation. This method is an informative option for assessing the quality of products at different stages of photodiode crystal manufacturing, which allows to estimate the density of surface states at the Si-SiO_2 interface [21, 22]. The absence of the need to measure the *C-V* characteristics is ensured by etching the mesa profile between the responsive elements and bleeding the crystal periphery, which completely removes the surface inversion layers that could contribute to the surface generation component of the dark current or worsen the insulation resistance between the active elements. In the case of the proposed mesa-photodiodes, only the Tamm and Shockley levels contribute to the dark current values. The only caveat is the lack of protective oxide on the surface of the etched areas, and therefore there is a need to seal the products without any delays, since the quasi-ideal surface after etching is very active and can oxidise even at room temperature or adsorb atoms, which will negatively affect the value of the density of surface states. Another way to ensure a low level of surface state density is to form silicon oxide or nitride on the surface of the etched areas using any known non-thermal method.

CONCLUSIONS

Silicon *p-i-n* mesa-photodiodes have been fabricated and studied. It is proposed to use a gold masking layer with an adhesive layer of chromium for chemical-dynamic polishing. The technology of mesa-photodiodes allows to exclude the first high-temperature oxidation from the technological cycle, which contributes to a decrease in the density of surface states at the Si-SiO_2 interface and reduces the degree of degradation of the electrophysical characteristics of silicon, which positively affects the parameters of photodiodes.

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ТЕХНОЛОГІЯ КРЕМНІЄВОГО *p-i-n* МЕЗА-ФОТОДІОДА

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У статті запропоновано технологію кремнієвих *p-i-n* меза-фотодіодів, яка дозволяє виключити одну високотемпературну операцію з технологічного маршруту. Зниження кількості термічних операцій дозволяє знизити міру деградації електрофізичних характеристик кремнію в процесі термообробок, що також сприяє зиженню густини поверхневих станів на межі розділу Si-SiO_2. Запропоновано проводи травлення меза-профілю методом хіміко-динамічного полірування з використанням золотого маскуючого покриття. Отримані фотодіоди є дешевшими, ніж серійні зразки виготовлені за дифузійно-планарною технологією та володіють вищою чутливістю.

Ключові слова: *кремній; фотодіод; чутливість; точковий дефект; дислокація; темновий струм*