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INVESTIGATION OF TEMPERATURE AND CHANNEL DIMENSION EFFECTS ON CMOS CIRCUIT PERFORMANCE

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This paper presents the impact of temperature variations and alterations in transistor channel dimensions on CMOS (Complementary Metal-Oxide-Semiconductor) circuit technology. To facilitate this investigation, we first identified critical parameters characterizing the device's performance, which could exhibit susceptibility to these influences. The analysis encompassed critical metrics such as the transfer characteristic, drain current, logic levels, inflection points, and truncation points. These parameters enabled us to validate the results obtained from the PSPICE simulator, which demonstrated unequivocal effectiveness. Notably, our simulation results unveiled significant effects resulting from a wide temperature range spanning from -100°C to 270°C, offering valuable in-sights into thermal-induced failures. Additionally, the influence of channel dimension changes on factors like drain current and transfer characteristics, as well as temporal parameters including signal propagation delay and rise and fall times, were meticulously examined and appreciated.
Key words: *CMOS; Channels dimensions; Temperature; PSPICE*
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1. INTRODUCTION

CMOS (Complementary Metal-Oxide-Semiconductor) technology stands as a cornerstone of modern electronics and integrated circuits, transforming the landscape of semiconductor electronics [1-2]. It has ushered in a new era of innovation, impacting the design and operation of electronic devices, from microprocessors in computers to sensors in smartphones and beyond [3]. At its core, CMOS leverages the unique properties of complementary transistor pairs, combining p-type and n-type transistors to create highly efficient and low-power digital logic circuits [4-5]. This complementary behavior results in minimal power consumption during idle states, rendering CMOS ideal for battery-powered and energy-efficient devices [6]. Beyond its energy efficiency, CMOS's scalability to ever-shrinking transistor sizes has been instrumental in advancing computational power in accordance with Moore's Law [7]. Furthermore, CMOS's reliability, noise immunity [8], and compatibility with various semiconductor materials have solidified its position as the backbone of the semiconductor industry [9-10]. The performance and behavior of CMOS devices and circuits are significantly affected by two pivotal factors: temperature and channel dimensions [11-12]. Precisely managing these variables is essential for optimizing integrated circuit operation, as they wield substantial influence over device characteristics, power consumption, and overall circuit performance [13]. Temperature exerts a profound impact on CMOS devices; as temperature rises, the electrical resistance of materials tends to decrease, affecting transistor performance [14-15]. Elevated temperatures can result in increased leakage currents in transistors, reducing efficiency and potentially compromising reliability [16]. Conversely, low temperatures can decelerate transistor response times [17]. To mitigate these effects, CMOS engineers must diligently implement thermal management techniques to ensure devices function within designated temperature ranges [18-19]. The dimensions of the transistor's channel region play a fundamental role in CMOS technology. Altering these dimensions can significantly impact transistor behavior. Scaling down channel dimensions, a common practice in advanced CMOS nodes, allows for greater transistor density on a single chip, enhancing computational power while reducing power consumption [20]. However, smaller dimensions introduce challenges, including increased leakage currents, short-channel effects, and variability in transistor performance [21]. Engineers must strike a delicate balance when resizing channel dimensions to ensure that the benefits of miniaturization outweigh the drawbacks [22-23]. Understanding the implications of temperature and channel dimensions on CMOS technology is imperative for optimizing the performance, power efficiency, and reliability of semiconductor devices. Engineers and researchers continually strive to discover innovative solutions to manage temperature effects and harness the advantages of altering channel dimensions as CMOS technology progresses [24].

This paper aims to investigate the impact of temperature and geometric alterations on CMOS inverter behavior. To facilitate this study, it is imperative to delineate the parameters that characterize device performance and exhibit susceptibility to these influences. The analysis will encompass key parameters, such as the transfer characteristic, drain current, logic levels, propagation delay, and rise and fall times.

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2. STATIC STUDY OF CMOS

2.1. DC results

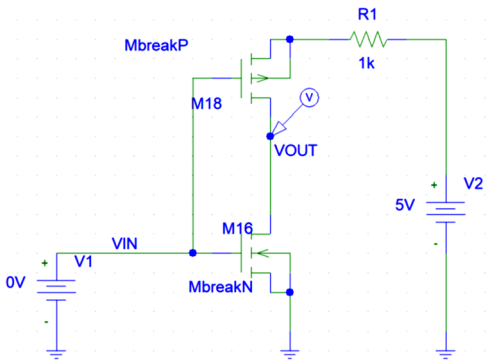

Figure 1. CMOS inverter circuit in static mode.

PSPICE empowers users to craft and virtually replicate electronic circuits within a computer-based environment, functioning as a robust framework for creating and assessing circuit diagrams [25]. It embraces a broad spectrum of circuit configurations, spanning analog and digital domains, thereby facilitating comprehensive scrutiny prior to any physical assembly. Users wield the flexibility to input component specifications, forge circuit connections, and apply voltage sources, thus enabling a profound analysis of circuit responses under diverse operational conditions [26]. PSPICE's capabilities extend to the simulation of transient reactions, the execution of steady-state AC assessments, and the exploration of diverse circuit attributes, thereby providing invaluable assistance in enhancing the comprehension of circuit behavior and performance [27]. To exemplify the utilization of the SPICE program, we have designed a CMOS inverter. In Figure 1, you can discern the incorporation of a DC input voltage spanning the range from 0V to 5V.

2.2. The transfer characteristic

As we sweep the input voltage, Vin, across a range from 0V to 5V, while keeping the inverter at its default operating conditions and an ambient temperature of 27°C, we observe a corresponding output voltage response that transitions from 5V to 0V. Notably, this voltage shift displays an inflection point precisely at the midpoint, where both input and output voltage levels equate to 2.5V, as visualized in Figure 2. Concurrently, the current flowing through the inverter, denoted as Id, exhibits a value of 60µA, illustrated in Figure 3.

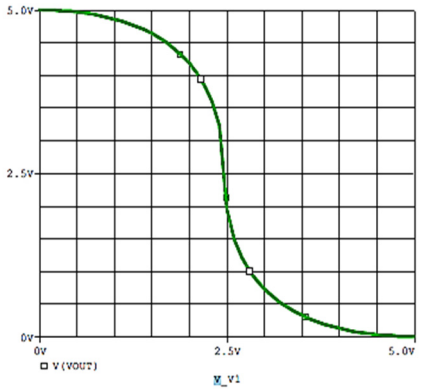

Figure 2. The transfer function Vout =f (Vin).

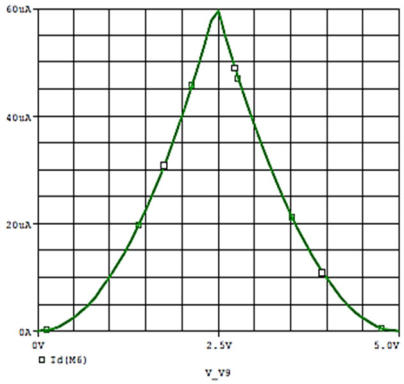

Figure 3. The drain current (Id) of CMOS.

2.3 The temperature effect on CMOS

2.3.1 The effect on the transfer function

When we adjust the temperature of the circuit, both below and above the ambient temperature of 27°C (Figure 4), as detailed in Table 1, we observe a subtle alteration in the transfer functions, where Vout is a function of Vin. This deviation is especially noticeable in the region where the NMOS transistor's behavior is prominent, differing notably from the reference curve indicated in green [28].

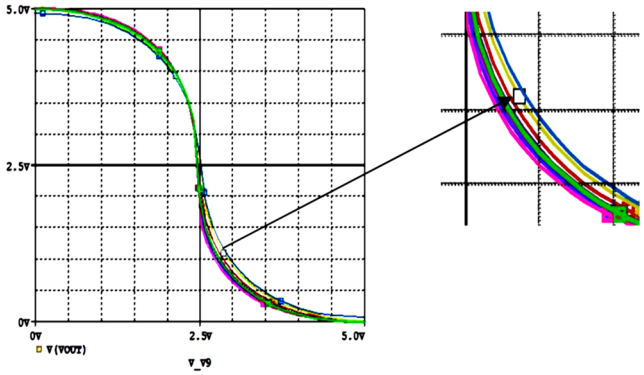

Figure 4. The temperature effect on the transfer function

Table 1. The difference in Idpeak variation as a function of temperature

Temperature (°C)	-100	-50	-20	0	27	50	100	200	270
Idpeak (µA)	118.51	84.353	72.496	66.357	59.558	54.804	46.814	36.42	44.316
ΔIdpeak(µA)	58.952	24.792	12.938	6.799	0	4.754	12.744	23.138	15.242

We note that the maximum drain current (Idpeak) varies with the variation in temperature with a significant difference.

2.3.2. The effect on the drain current:

As depicted in Figure 5, an interesting trend becomes apparent: the peak current, Idpeak, exhibits an inverse relationship with temperature. When the temperature decreases, Idpeak increases, and vice versa. Remarkably, the shape of this relationship remains consistent, with the peak current consistently centered around a voltage Vgs of 2.5V [29]. It's worth noting an exception to this pattern, occurring at the extreme temperature of T = +270°C, where the curve originates with an initial current, Id0, measuring 13.755µA. This initial current serves as the starting point for calculating the incremental changes, as documented in Table 1.

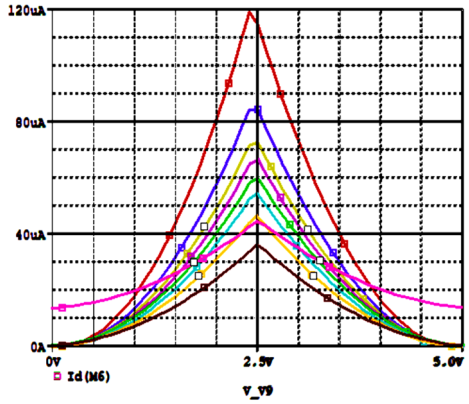

Figure 5. The temperature effect on the drain current.

2.4. The effect of geometric alteration on CMOS

2.4.1. The effect on the drain current

By altering the dimensions of the NMOS transistor channel, specifically the length (referred to as "L") and the width (referred to as "W"), we can observe corresponding variations in two critical parameters: the peak current, Idpeak, and the inflection point. These changes are visually represented in Figures 6 and 7, and their precise values are documented in Table 2 for reference [30].

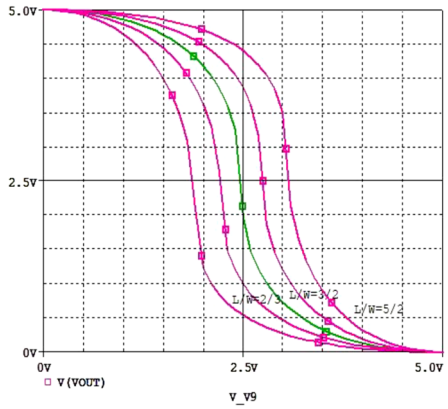

Figure 6. The transfer function Vout =f (Vin)

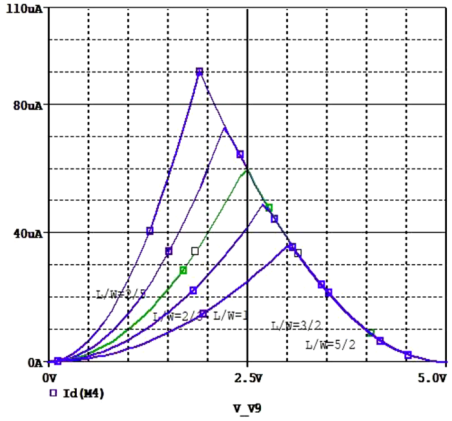

Figure 7. The drain current (Id) of CMOS.

The alteration of the dimensions, namely the width and length, of the NMOS transistor channel has a notable impact on the transfer function of the CMOS circuit. It's evident that this influence causes a lateral shift in the output signal curve (Vout = f(Vin)) when compared to the reference signal (depicted as the green curve) [31]. Specifically, an increase in the width-to-length ratio of WN/LN prompts the curve to shift to the left of the reference, while a decrease in this ratio results in a shift to the right [32]. This shift of the curve corresponds to changes in the inflection point, leading to slight differences in the values of the truncation points, which are detailed in Table .2. Additionally, we observe a noteworthy pattern in the behavior of the maximum drain current, Idpeak. As the WN/LN ratio increases, Idpeak also experiences an increase, and its curve shifts to the left of the reference [33]. Conversely, a decrease in the WN/LN ratio causes Idpeak to decrease, and

its curve shifts to the right relative to the reference curve. This further highlights the significance of the WN/LN ratio in shaping the performance characteristics of the CMOS circuit [34].

Table 2. The maximum drain current Idpeak and the inflection point variation as a function of geometric alteration.

WN/LN	2/5	2/3	1	3/2	5/2
Idpeak (µA)	36.00	48.60	59.559	72.60	90.25
Inflection point (V)	(3.1;2.5)	(2.7;2.5)	(2.5;2.5)	(2.2;2.5)	(1.9;2.5)

2.4.2. Change in PMOS

By adjusting the dimensions of the channel in the PMOS transistor, specifically its length ("L") and width ("W"), we can observe corresponding alterations in two key parameters: the peak current (Idpeak) and the inflection point. These variations are visually represented in Figures 8 and 9, and their precise values are documented in Table 3 for reference. To explain further, changing the dimensions of the PMOS transistor channel influences the behavior of the circuit. This leads to shifts in the curve representing the circuit's output signal (Vout = f(Vin)) concerning the reference signal [35]. The direction of this shift depends on whether the width-to-length ratio (WP/LP) increases or decreases [36]. These shifts correspond to changes in the inflection point and may result in minor differences in the values of the truncation points. This data is detailed in Table 3.

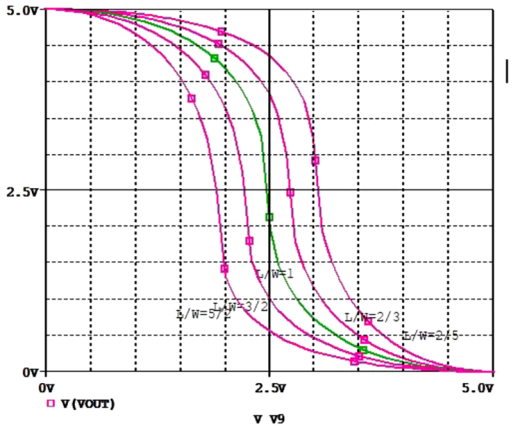

Figure 8. The transfer function Vout =f (Vin)

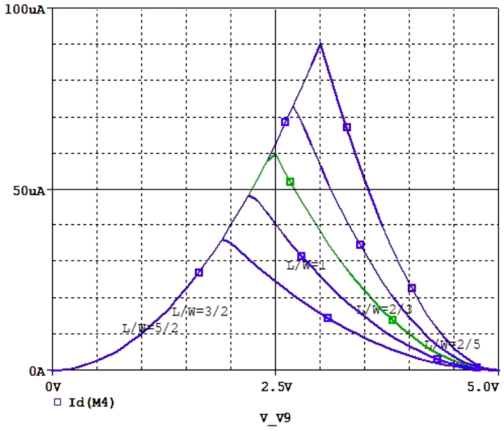

Figure 9. The drain current (Id) of CMOS

As we modify the dimensions of the PMOS transistor channel, specifically the length (LP) and width (WP), a significant influence becomes evident. When we decrease the width-to-length ratio (WP/LP) by a factor of 1, there is a discernible shift in the output signal curve (Vout = f(Vin)) to the left compared to the reference curve [37]. This shift in position includes variations in the location of the inflection point, which can change under different conditions, or it may shift back towards the right. Additionally, this adjustment also impacts the positions of the high and low truncation points. What's particularly interesting is the behavior of the maximum drain current (Idpeak). When the WP/LP ratio increases, Idpeak experiences an increase, but this time, its curve shifts to the right relative to the reference. Conversely, a decrease in the WP/LP ratio by 1 results in a decrease in Idpeak, and the curve shifts left, in contrast to the behavior of the NMOS transistor. This observation underscores the inverse relationship between the WP/LP ratio and the behavior of PMOS and NMOS transistors [38].

Table 3. The maximum drain current Idpeak and the inflection point variation as a function of geometric alteration.

WN/LN	2/5	2/3	1	3/2	5/2
Idpeak (µA)	36.10	48.40	59.558	72.90	90.00
Inflection point (V)	(1.9;2.5)	(2.2;2.5)	(2.5;2.5)	(2.7;2.5)	(3.1;2.5)

2.4.3. Change in NMOS and PMOS

When we concurrently vary the dimensions of both the NMOS and PMOS transistors' channels, including their lengths (LN and LP) and widths (WN and WP), a distinct phenomenon emerges in contrast to the previous scenarios. Notably, the maximum drain current, Idpeak, for the CMOS inverter consistently decreases as these dimensions are altered. However, this decrease is accompanied by a shift in the Idpeak curve to the right of the reference curve if the ratio βN/βP decreases by 1, and to the left if it increases. Furthermore, the curve representing the output voltage (Vout = f(Vin)) also undergoes shifts when βN/βP is modified [39]. If βN/βP increases, the curve shifts to the left of the reference, and conversely, it moves back to the right. These shifts affect the inflection point, as well as the high and low truncation points, all while preserving the characteristic shape of the curve, with no deformations. This phenomenon indicates that each transfer function has a distinct threshold in comparison to the others due to the varying size ratio of the PMOS and NMOS transistors, βN/βP, in different transfer functions [40]. As this ratio increases, the threshold of the CMOS inverter decreases, influencing its performance characteristics (Figures 10 and 11).

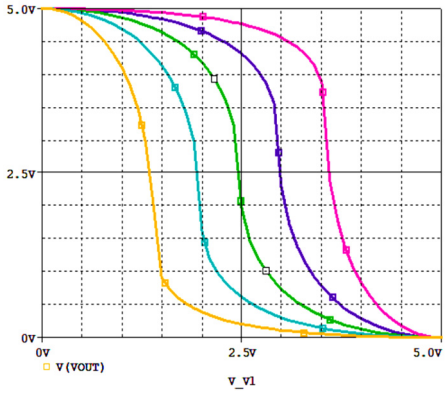

Figure 10. The transfer function Vout =f (Vin)

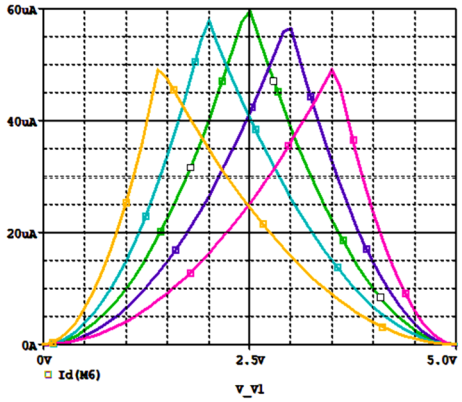

Figure 11. The drain current (Id) of CMOS

Table 4. The maximum drain current Idpeak, the inflection points and truncation points variation as a function of geometric alteration

βN = WN/LN	2/5	2/3	2/5	1	3/2	3/2	5/2
BP = WP/LP	5/2	3/2	2/5	1	3/2	2/3	2/5
βN/βP	0.16	0.44	1	1	1	2.25	6.25
Idpeak (µA)	49.00	56.64	59.56	59.56	59.56	57.714	49.00
Inflection point (V)	3.60	2.99	2.5	2.5	2.5	1.94	1.35
Maximum truncation point (V)	(3.21;4.40)	(2.5;4.31)	(1.7;4.5)	(1.7;4.5)	(1.7;4.5)	(1.16;4.56)	(0.58;4.75)
Minimum truncation point (V)	(4.24;0.42)	(3.72;0.52)	(3.10;0.63)	(3.10;0.63)	(3.10;0.63)	(2.62;0.61;)	(1.71;0.60)

3. DYNAMIC STUDY OF CMOS

3.1. Simulation circuit

To further investigate this study, we utilized the PSPACE design program to conduct experiments with a CMOS inverter. These experiments involved applying an AC input voltage spanning from 0V to 5V, as visually represented in the Figure 12.

3.2. The default output signal

Throughout these simulations, a constant temperature of 27 °C was maintained, and the CMOS configuration remained at its default state, with a width-to-length ratio (W/L) of 1. It's important to note that we employed an inverted CMOS circuit, which means that the output response exhibits an inversion compared to the input signal. The input signal is represented by the red curve, while the green curve corresponds to the output signal (Figures 13).

3.2.1. Rise times and propagation delays:

During signal transitions in a circuit, both the NMOS and PMOS transistors conduct simultaneously, resulting in increased power dissipation. The dissipation is most pronounced when both transistors reach the saturated state, which is undesirable due to the elevated power consumption. To mitigate this issue, it is essential to enhance the rise and fall times of the signals, which are the durations taken for the transitions from low to high and high to low states, respectively. Reducing these times helps minimize power dissipation during transitions [41]. Additionally, the propagation delay, which represents the time it takes for an input change to affect the output, is a critical parameter that needs careful consideration as it significantly impacts the circuit's overall performance and efficiency (Figure 14).

3.3 The temperature effect

In our exploration of temperature's influence on CMOS, we systematically manipulated temperature settings across a wide range, encompassing temperatures from -100°C to the maximum temperature at which CMOS exhibits a reaction, 270°C, as depicted in Figure 15. The impact of temperature on CMOS performance is indeed significant. To illustrate, in terms of propagation delay, a clear trend emerges: higher temperatures correspond to reduced propagation delays, while lower temperatures lead to their increase. Similarly, when considering the rise and fall times of signals, elevated temperatures prompt shorter times, implying faster transitions between logic levels. This phenomenon is likely attributed to an enhancement in carrier mobility, facilitating the swifter movement of charges within the transistors [42]. Conversely, lower temperatures extend the rise and fall times, resulting in slower transitions. This can be attributed to a reduction in carrier mobility under colder conditions.

3.4. The effect of geometric factors (W and L)

3.4.1. Change in NMOS

In Figure 16, we observe the impact of altering the geometric characteristics (specifically, the width, W, and length, L) of the NMOS transistor on the behavior of the CMOS inverter. Notably, an increase in the size of the NMOS

transistor, indicated by a higher W/L ratio, has a beneficial effect on the circuit. It reduces the propagation delay, enhancing the inverter's speed. Additionally, with respect to rise and fall times, an increase in the W/L ratio of the NMOS transistor leads to shorter rise and fall times for signals [43]. This implies that transitions between logic levels occur more swiftly, contributing to improved overall performance.

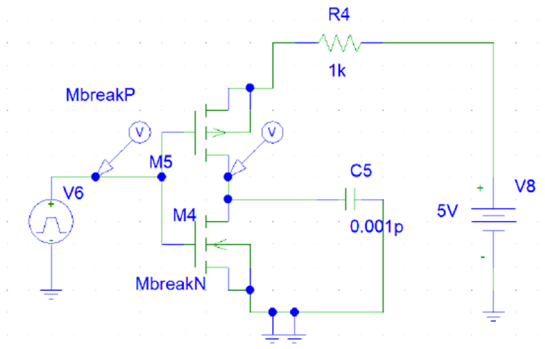

Figure 12. CMOS inverter circuit in dynamic mode

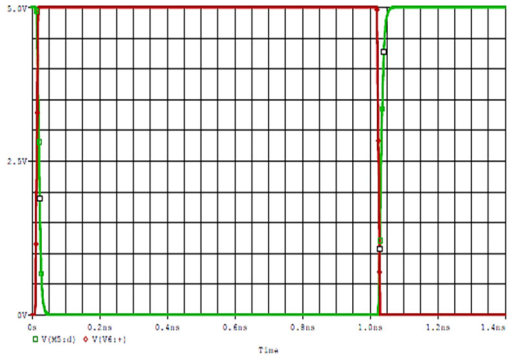

Figure 13. Default input and output signals of CMOS inverter

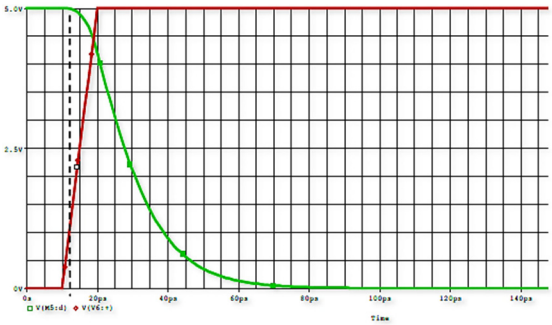

Figure 14. Rise times and propagation delays of CMOS inverter

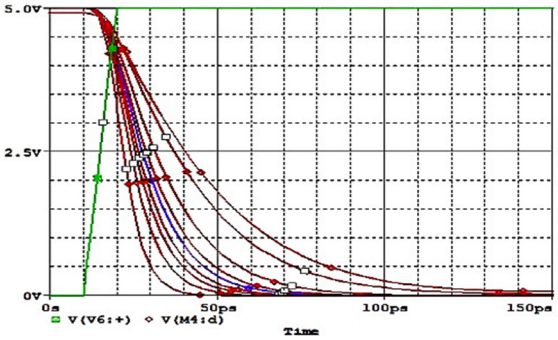

Figure 15. The temperature effect on CMOS

3.4.2. Change in PMOS

As demonstrated in Figure 17, we investigate the influence of altering the geometric parameters (specifically, the width, W, and length, L) of the PMOS transistor on the CMOS inverter. Upon careful examination of the graphical results, it becomes evident that the PMOS geometric factors (W and L) exhibit no discernible impact on the CMOS inverter concerning key performance aspects such as propagation delay and rise/fall times. In other words, variations in the PMOS transistor's geometric characteristics do not yield significant changes in these parameters.

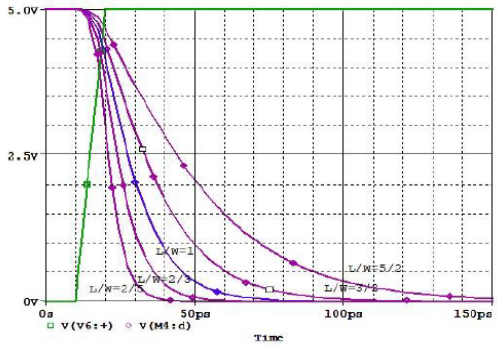

Figure 16. The change in NMOS geometric factors effect on CMOS

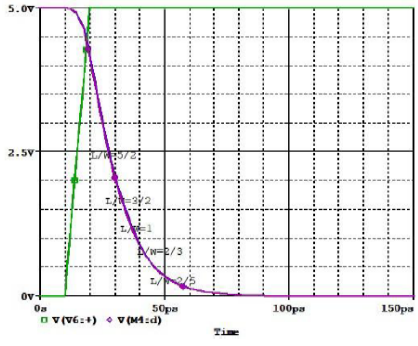

Figure 17. The change in PMOS geometric factors effect on CMOS.

3.4.3. Change in NMOS and PMOS

Figure 18 provides a comprehensive visual representation of the impact of altering both NMOS and PMOS transistor geometric parameters, specifically width (W) and length (L), on the CMOS inverter. A notable observation emerges: the geometric characteristics of the NMOS transistor play a pivotal role in influencing the temporal parameters of the CMOS circuit, while the geometric factors of the PMOS transistor do not appear to have a discernible effect on CMOS [44].

Consequently, the curves depicted in Figure 18 closely resemble those in Figure 16, reinforcing the notion that the NMOS transistor's geometric attributes are the primary drivers of temporal changes in the CMOS inverter.

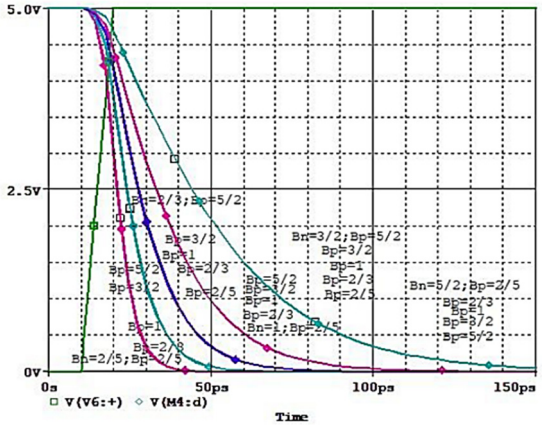

Figure 18. The change in NMOS and PMOS geometric factors effect on CMOS

4. CONCLUSION

In summary, this study investigates the impact of temperature variations and alterations in transistor channel dimensions on CMOS (Complementary Metal-Oxide-Semiconductor) circuit technology. To facilitate this investigation, we first identified critical parameters characterizing the device's performance, which could exhibit susceptibility to these influences. The analysis encompassed critical metrics such as the transfer characteristic, drain current, logic levels, inflection points, and truncation points. These parameters enabled us to validate the results obtained from the PSPICE simulator, which demonstrated unequivocal effectiveness. Notably, our simulation results unveiled significant effects resulting from a wide temperature range spanning from -100°C to 270°C, offering valuable in-sights into thermal-induced failures. Additionally, the influence of channel dimension changes on factors like drain current and transfer characteristics, as well as temporal parameters including signal propagation delay and rise and fall times, were meticulously examined and appreciated

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ДОСЛІДЖЕННЯ ВПЛИВУ ТЕМПЕРАТУРИ ТА РОЗМІРІВ КАНАЛУ НА ПРОДУКТИВНІСТЬ СХЕМИ CMOS

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У цьому дослідженні представлено вплив коливань температури та змін розмірів каналу транзистора на технологію CMOS (комплементарний метал-оксид-напівпровідник). Щоб полегшити це дослідження, ми спершу визначили критичні параметри, що характеризують продуктивність пристрою, які можуть бути чутливими до цих впливів. Аналіз охоплював критичні показники, такі як характеристика передачі, струм витоку, логічні рівні, точки перегину та точки зрізання. Ці параметри дозволили нам підтвердити результати, отримані від симулятора PSPICE, який продемонстрував однозначну ефективність. Примітно, що результати нашого моделювання виявили значні ефекти, що є наслідком широкого діапазону температур від -100°C до 270°C, пропонуючи цінну інформацію про несправності, спричинені нагріванням. Крім того, було ретельно вивчено та оцінено вплив змін розміру каналу на такі фактори, як струм стоку та характеристики передачі, а також часові параметри, включаючи затримку поширення сигналу та час наростання та спаду.

Ключові слова: *КМОП; розміри каналів; температура; PSPICE*