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# ON THE PROPERTIES OF THE $Si$-$SiO_2$ TRANSITION LAYER IN MULTILAYER SILICON STRUCTURES

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Capacitance spectroscopy was used to study the capacitive-voltage characteristics of multilayer structures with a $Si$-$SiO_2$ transition layer in $Al$-$SiO_2$-n-$Si$ type samples fabricated by the thermal oxidation of a semiconductor. It is shown that the inhomogeneous distribution of the density of surface states is a localized electroactive center at the very semiconductor-dielectric interface, due to over-barrier charge emission or thermal ionization of impurity centers.
**Keywords:** *MDS structure; Silicon; Transition layer; Interface; Temperature; Dielectric layer*
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## INTRODUCTION

An integral part of most modern semiconductor devices is silicon MDS or MOS structures. Given that the physical processes occurring on the semiconductor-insulator transition layer have a significant impact on the performance of semiconductor devices. Layers of amorphous silicon dioxide grown on silicon by thermal oxidation satisfy most of the requirements listed above. At the same time, the technological modes of its production easily fit into the existing technological processes for the production of semiconductor devices and integrated circuits. The foregoing made $SiO_2$ films the most common material for creating passivating and insulating layers in semiconductor instrumentation. Analysis of the dielectric and transition layers of $Si$-$SiO_2$ may eventually prove useful for constructing theoretical or computer simulations of impurity states [1,12]. To solve it, it is necessary to have information about the nature of electron and hole trapping centers (trapping centers). One of the important features of semiconductors is that their electrical and optical properties can differ significantly depending on the state of the surface and change with its various processing (grinding, etching), and changes in environmental parameters. The common cause of these phenomena is that in a limited crystal there arise not only quantum states of electrons moving in the bulk of the crystal, but also additional states in which the electrons are localized on the very surface of the crystal. Accordingly, in addition to the volume energy levels that form the energy zones of an infinite crystal, there appear local energy levels located near the surface itself [1,2,13].

The presence of local surface energy levels leads to the fact that electrons and holes can "stick" to the surface, forming a surface electric charge. In this case, an induced charge equal in magnitude and opposite in sign appears in the volume under the surface, i.e. enriched or depleted near-surface layers appear. The appearance of such layers explains the influence of the surface on the equilibrium properties of semiconductors (electrical conductivity, work function, contact potential difference, etc.). Based on these results, our goal is to obtain cheap microchips.

## MATERIALS AND METHODS

To experimentally study the effect of $Si$-$SiO_2$ transition layers on the capacitance-voltage characteristics in three-layer structures, we used the most widely used in microelectronics metal-dielectric-semiconductor structures of the $Al$-$SiO_2$-n-$Si$ type, fabricated by the thermal oxidation of silicon KEF-5 with crystallographic orientation < 100>. To form MDS structures, aluminum field electrodes 0.8 mm in diameter were deposited on the $SiO_2$ film by thermal deposition in vacuum. The contact to the semiconductor substrate was also made of aluminum. For comparison, different methods were used [2,3,14] and to study the effect of transition layers, measurements of capacitance-voltage characteristics were carried out (Fig. 1). Measurements of the dielectric constant were carried out in the range from 30ºC to 200ºC and a voltage sweep in the range from -10 to 8 V. The films have a specific resistance $\rho = 10^{13}\ldots10^{16}$ Ohm cm, a breakdown field strength $E = (1\ldots3)\ 10^6$ V/cm . The value of the relative permittivity for different layers $\varepsilon = 5\ldots12$.

## RESULTS AND DISCUSSION

The obtained characteristics strongly depend both on the technological regimes for the manufacture of layered structures and on the impurity content in the starting materials. It is shown that the best characteristics are achieved at an annealing temperature from 650ºC to 900ºC, but for a dielectric, the tangent of the angle increases to 0.1, but the insulating properties of the films also deteriorate. These data are also confirmed by the results obtained by other authors [4-6].

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On the whole, the Si-$SiO_2$ structure is characterized by the presence of mechanical stresses in it. Mechanical stresses already arise in a non-oxidized silicon wafer during processing of its upper and lower surfaces in different ways. In the case of growing oxide on one of the surfaces of a semiconductor wafer, mechanical stresses can be significant. This is primarily due to the difference (almost an order of magnitude) in the coefficient of linear expansion of silicon materials, since the oxide film is grown (or deposited) at an elevated temperature. The cooling of the Si-$SiO_2$ structure leads to the appearance of mechanical stresses, and, consequently, causes deformation of the structure (the $SiO_2$ film is compressed, and the surface part of the Si plates is stretched). The cause of the occurrence of mechanical stresses can also be the difference in the structure of the materials of the semiconductor and dielectric.

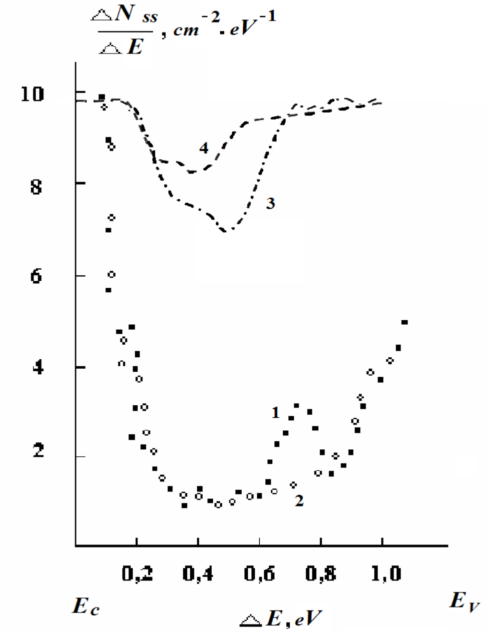


**Figure. 1.** Capacitance-voltage characteristics of 1 - Si, 3 - $SiO_x$, 2 – 4 after TA

Let us briefly consider the main characteristics of the semiconductor-insulator transition layer. The capacitance-voltage characteristics of MDS structures with Si-$SiO_2$ transition layers do not differ significantly from the C-V characteristics for silicon. From a comparison of the obtained C-V characteristics with the calculated one, the surface charge Q and the density of surface states Nss at the semiconductor-dielectric interface were determined (Fig. 2). For our structures obtained at a temperature of about 200ºC, the minimum density Nss for the <100> silicon orientation was $\approx 2 \cdot 10^{10}$ $cm^{-2}$ $eV^{-1}$, and for <111> Nss $\approx 1.2 \cdot 10^{10} cm^{-2}$ $eV^{-1}$. Such differences in the values of Nss are explained by different values of the activation energy and the number of free bonds of atoms for different orientations of the crystal surface [7,15].

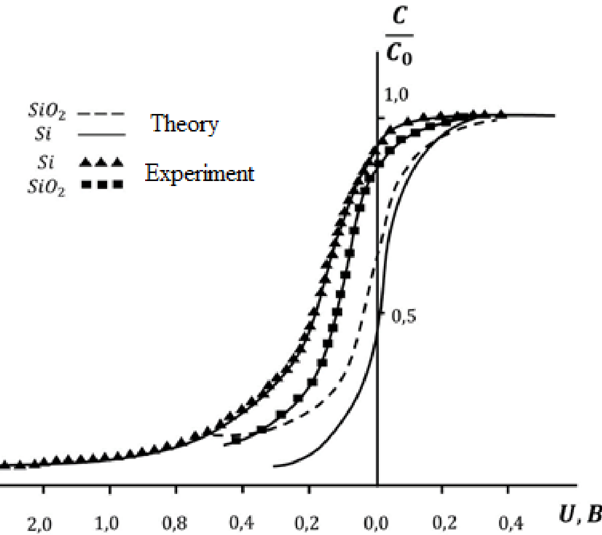


**Figure. 2.** Theoretical and experimental capacitance-voltage characteristics of silicon structures normalized to the capacitance value of the dielectric layer

Comparative detailed analysis of the theoretical and experimental methods showed that the formulation of the density of surface states near the inversion region of the C-V characteristics, as well as not far from the region of strong enrichment. To describe the properties of the interface, the three-layer model is most often used [6.9], in which the semiconductor-dielectric system is divided into three regions qualitatively different in their properties: the region of regular $SiO_2$ and single-crystal Si, the transition region of the non-stoichiometric composition of $SiO_2$ and the regions of deformed $SiO_2$ attached to it and cushioned Si [1,10]. The thickness of the $SiO_2$ layer is 0.6 ÷ 2 µm and depends on the pre-treatment of the silicon substrate and the oxidation mode. The disordered layers of Si and $SiO_2$ applied to this region are characterized by an increased content of various kinds of defects and mechanical stresses caused by different coefficients of thermal expansion of the $SiO_2$ layer and the silicon substrate [8,16]. It is the region of the nonstoichiometric composition of $SiO_2$ and the regions of disordered $SiO_2$ and Si adjacent to it that in this model are united under the concept of an interface, and the defects contained in these regions determine its electrophysical characteristics. [6,11]. The energy state density distributions at the Si-$SiO_2$ interface over the band gap of silicon are shown in Fig.3. As for Si-$SiO_2$ structures, the density of states is minimal near the middle of the band gap and increases near the edges of the C- and V- bands. The value of the maximum density Nss, in accordance with [3,17], depends both on the orientation of the substrate and on the conditions for obtaining the dielectric layer.

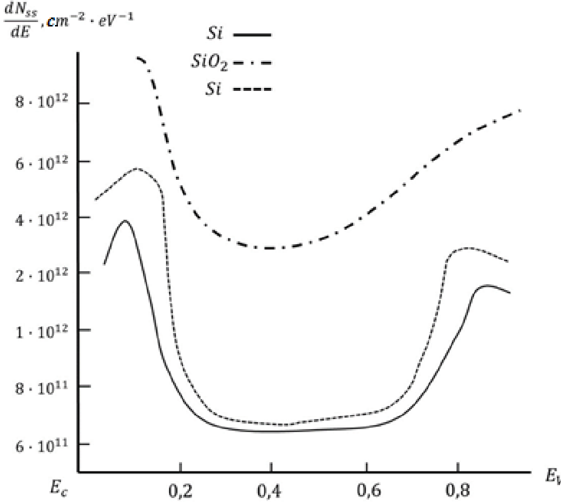


**Figure 3.** Sample-averaged distribution of the density of surface states over the band gap of a semiconductor and dielectric

It can be seen from the figure that the smallest scatter of the obtained data takes place in the energy range from $E_c$ - 0.2 eV to $E_c$ - 0.75 eV. Significant scatter of values for MIS structures, fabricated and previously obtained results [3,11]. This, according to the authors of [5,6], is a consequence of optical inactive oxygen and the presence of local spatial inhomogeneities in the distribution of the surface charge on the Si – $SiO_2$ transition layer and the fluctuations of the surface potential associated with them. It is in this energy range that a good uniformity of the results of all measurements is observed. Meanwhile, a rather large spread in the values of the averaged values of the density of surface states near the edges of the energy bands is synchronously observed. It is possible that from Figure 3, in the energy range from $E_c$ to $E_c$-0.2 eV and from $E_c$-0.75 eV to $E_v$, this spread reaches 30%. In our opinion, the reason for this scatter of data may be as follows. As the enrichment voltage applied to the structure decreases, the electrons localized on the surface states begin to be ejected into the conduction band due to thermal generation. In this case, the probability of their recapture is high, since the concentration of electrons near the interface is rather high [3,8].

## CONCLUSIONS

From the experimentally observed characteristics, an important point here is the way holes appear in the dielectric, since the heights of the Al-$SiO_2$ and Si-$SiO_2$ barriers are large in order to appear by hole tunneling. Consequently, the center localized on the semiconductor-insulator transition layer itself is responsible for the inhomogeneous distribution of the density of surface states. As for Si-$SiO_2$ elements, this is typical for electrical conductivity due to above-barrier charge emission or thermal ionization of impurity centers [11,18]. In the absence of voltage on the structure and at low depleting voltages, the indicated center is neutral. At sufficiently high inversion voltages, the center is ionized, releasing electrons localized on it, which are captured by the charge of the inversion layer, reducing the rate of its formation. With full ionization of the center, the charge of the inversion layer increases due to the thermal generation of minor charge carriers, which leads to a further decrease in the measured capacitance of the structure [8,19,20]. Based on the above, it can be assumed that the experimentally observed, dielectric parameters of the Si-$SiO_2$ elements studied by us are close to the characteristics of silicon MDS structures, and even better in a number of parameters. The low-temperature technology for producing oxide films makes it possible to use these materials to create MIS structures based on multicomponent semiconductors, for which high-temperature treatment is undesirable.

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**ПРО ВЛАСТИВОСТІ ПЕРЕХІДНОГО ШАРУ Si-$SiO_2$ У БАГАТОШАРОВИХ КРЕМНІЄВИХ СТРУКТУРАХ**

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Методом ємнісної спектроскопії досліджено вольт-ємнісні характеристики багатошарових структур з перехідним шаром Si-$SiO_2$ у зразках типу Al-$SiO_2$-n-Si, виготовлених термічним окисленням напівпровідника. Показано, що неоднорідний розподіл щільності поверхневих станів є локалізованим електроактивним центром на самій межі розділу напівпровідник-діелектрик внаслідок надбар’єрної емісії заряду або термічної іонізації домішкових центрів.

**Ключові слова:** *структура MDS; кремній; перехідний шар; інтерфейс; температура; діелектричний шар*