ISOLATION OF RESPONSIVE ELEMENTS OF PLANAR MULTI-ELEMENT PHOTODIODES†

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In the mass production of multi-element silicon p-i-n photodiodes, the problem of systematic rejection of products due to a decrease in the insulation resistance between the active elements of photodetectors has been revealed. The purpose of this work is to study the causes of insulation resistance degradation and to establish optimal methods for avoiding this phenomenon. A comparative analysis of three insulation methods was carried out: classical insulation by the surface of a non-conductive substrate and a dielectric layer; insulation by means of mesaprofile grooves with a dielectric film; insulation by means of areas of limitation of surface leakage channels isotypic with the substrate material (in this case, p-type) formed in the gaps between active elements. The study found that the reason for the deterioration of the insulation resistance between the active elements of photodiodes is the presence of conductive inversion channels at the Si-SiO2 interface due to the use of silicon with high resistivity. One mechanism for the formation of inversion channels is the redistribution of impurities in the masking oxide (in particular, phosphorus) and their diffusion to the interface during thermal operations. Another mechanism for the formation of inversion layers is the diffusion of boron from silicon into SiO2 during heat treatment due to the fact that the boron segregation coefficient is less than one. In the manufacture of samples with insulation using non-conductive areas of the substrate, a decrease in insulation resistance was observed as the technological route was performed (after each subsequent operation, the resistance degraded). The degree of degradation can be reduced by reducing the duration of thermal operations. It has been shown that reducing the thickness of the masking oxide causes a decrease in insulation resistance. When using mesa-technology, it is possible to increase the insulation resistance by eliminating the high-temperature oxidation operation and, in fact, due to the absence of a masking coating during phosphorus deposition. Insulation by means of p-type areas in the gaps between the active elements allows to obtain the highest insulation resistance values. The formation of these regions with a width of 100 μm in the gaps with a width of 200 μm allowed us to obtain an insulation resistance of 25-30 MΩ. To ensure the insulation of the active elements of photodiodes by this method, two thermal operations are added to the technological route. The number of thermal operations can be reduced by doping the entire silicon surface with a low boron concentration before forming a masking coating.

Keywords: Silicon; Photodiode; Insulation resistance; Silicon oxide; Inversion layer

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An important task of modern photoelectronics is to detect the coordinates of objects in space. Usually, multi-element coordinate photodiodes (PD) are used in coordinate determination systems. The coordinate PD is usually a two- or four-element photodiode on one semiconductor plate, in which the responsive elements (RE) are separated by gaps smaller than the size of the light probe [1]. To ensure the high responsibility of the used photodetectors, a high-resistance material is used. When we serially manufactured coordinate silicon PDs, we saw a slight decrease in the insulation resistance between the REs, and in the case of the production of the PDs with a guard ring (GR), a decrease in the insulation resistance between the REs and the GR was also observed. This contributed to the growth of the dark currents of the photodiodes by this method, two thermal operations are added to the technological route. The number of thermal operations can be reduced by doping the entire silicon surface with a low boron concentration before forming a masking coating.

When reviewing the literature, it was seen that most of the works are devoted to the methods of isolation of integrated circuits (ICs). Thus, methods of isolation of IC elements allow to manufacture devices on conductive and non-conductive substrates. On the conductive substrate, the insulation of the IC elements is carried out by a p-n-junction and a thin dielectric film, and on the non-conductive one by insulation with air gaps and dielectric materials [5]. In particular, [6] describes the principle of isolation of active IC elements using the isoplanar method. The method is combined. In this technology, the insulation of the vertical walls of the components is carried out by a thick layer of silicon dioxide, which extends from the surface of the epitaxial layer to the n+ hidden layer; the isolation of the bottom part of the components is carried out by a reverse-biased p-n-junction. Another combined method of isolation of IC elements is epiplanar [7]. It was implemented after the development of local epitaxial growth of silicon on certain areas of the substrate surface. The method of selective epitaxial growth of silicon allows the formation of IC components, providing self-connection of isolated regions and the n+ hidden layer. One of the new "exotic" insulation methods is the IPOS technology - insulation with oxidized porous silicon. In this technological method, two main processes can be distinguished. The first is a selective

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Isolation of Responsive Elements of Planar Multi-Element Photodiodes

The isolation of responsive elements of planar multi-element photodiodes is a critical aspect in ensuring proper insulation resistance among the active elements. The presence of pores and strongly developed surfaces in the treated area can affect the insulation resistance of the photodiodes. When specific processing methods are applied, silicon regions are isolated from the sides using mesa-profile grooves filled with polycrystalline silicon. This method, known as V-ATE (vertical anisotropic etch), is used for isolating photodiode structures. It allows for the formation of V-shaped grooves filled with polycrystalline silicon, which is a variant of the method of combined isolation of components, in which the separation tracks are not filled with silicon dioxide or other insulating materials.

Ensuring proper insulation resistance of multielement photodetectors is crucial for preventing degradation between active elements. Classical planar structures are usually insulated using silicon oxide films formed in a single technological process with diffusion of acceptors or donors or silicon nitride films. V-ATE technology (V-ATE - vertical anisotropic etch) is available as a variant of the method of combined isolation of components, in which the separation tracks are not filled with silicon dioxide or other insulating materials.

To study the insulation methods and establish optimal technological options, the authors of the paper decided to investigate the influence of the isolation methods of REs based on silicon four-element p-i-n PDs with a guard ring. The production process was carried out using diffusion-planar technology according to the technological modes of diffusion processes given in [15]. The starting material was single-crystal dislocation-free p-type silicon with orientation [111], p=17-20 kΩ cm.

The authors considered the resistance between all REs and GR (Rcon) as a parameter that allows them to evaluate the degree of insulation of active elements. Determination of Rcon was carried out according to the method given in [1] with Ubias=2 V and load resistance RL=10 kΩ.

A comparative analysis of three methods of isolation was carried out: classical – isolation with the surface of a conditionally non-conductive substrate and a dielectric layer (PD1) (Fig. 1); isolation using mesa-profile grooves with a dielectric film (similar to the V-ATE method) (PD2); and isolation using anodic dissolution of silicon in hydrofluoric acid, in which porous silicon is formed in the treated area. The second is heat treatment in an oxidizing environment, in which porous silicon oxidizes at a high rate due to the presence of pores and strongly developed surface. As a result of such selective processing, porous silicon regions are isolated from the sides by silicon dioxide. At this, unlike isoloplanar technology, it is excluded in this case the need for long-term high-temperature oxidation.

There are also methods of isolating IC elements using etched grooves on the surface of the substrates. In particular, insulation using V-grooves, filled polycrystalline silicon (VIP-method, VIP-V-brave isolation polisilicon) is based on vertical anisotropic etching of silicon substrates with formation of V-shaped grooves filled with polycrystalline silicon [9, 10]. V-ATE - technology (V-ATE - vertical anisotropic etch) is also available as a variant of the method of combined isolation of components, in which the separation tracks are not filled with silicon dioxide or other insulating materials.

Photodiodes with a mesa structure (Fig. 3) were manufactured according to the following technological route: predeposition of phosphorus to the front side to create n-type layer, etching the grooves of the mesa profile by the method of chemical dynamic polishing [16] to obtain REs (Fig. 4-1) and GR (Fig. 4-2), driving-in of phosphorus in an oxygen atmosphere to redistribute the alloying impurity, increase the depth of the n-p junction and form an anti-reflective coating (Fig. 4-4); diffusion of boron to the reverse side of the substrate to create a p-type ohmic contact (Fig. 4-8); photolithography for creating contact windows; sputtering of Cr-Au on the front and back sides (Fig. 4-5 and 6).

**EXPERIMENTAL**

It was decided to investigate the influence of the isolation methods of REs based on silicon four-element p-i-n PDs with a guard ring. Production was carried out using diffusion-planar technology according to the technological modes of diffusion processes given in [15]. The starting material was single-crystal dislocation-free p-type silicon with orientation [111], p=17-20 kΩ cm.

We will consider the resistance between all REs and GR (Rcon) as a parameter that allows us to evaluate the degree of insulation of active elements. Determination of Rcon was carried out according to the method given in [1] with Ubias=2 V and load resistance RL=10 kΩ.

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Photodiodes with surface leakage restriction channels isotypic with the substrate material (Fig. 5) were manufactured according to the following technological route: oxidation of silicon substrates to obtain a masking coating; photolithography for the formation of windows for boron diffusion; diffusion of boron to the front side of the crystal to obtain a \( p^+ \)-region; oxidation/boron driving-in to mask the \( p^+ \)-layer and increase the depth of the \( p^+ -p^- \)-junction; photolithography for the formation of windows for phosphorus diffusion; diffusion/predeposition of phosphorus to obtain \( n^- \)-type REs and GR; phosphorus driving in to increase the depth of the \( n^- -p^- \)-junction and the formation of anti-reflective \( \text{SiO}_2 \); diffusion of boron to the rear side of the substrate to create an ohmic \( p^+ \)-layer and heterization of generation-recombination centers. A schematic cross-section of the PD2 crystal can be seen in Fig. 6.

RESULTS OF THE RESEARCH AND THEIR DISCUSSION

A) Mechanisms of insulation resistance degradation.

It should be noted that one of the mechanisms for the formation of conductive inversion channels at the Si-SiO\(_2\) interface and the reduction of insulation resistance between active elements is the redistribution of impurities in the masking oxide (including phosphorus) and their diffusion to the interface of the two phases during thermal operations, respectively, with an increase in the total duration of thermal operations, it is possible to doping of impurities in the silicon surface through the masking SiO\(_2\) [17]. Therefore, in the formation of masking coatings, it is necessary to take into account not only the thickness of the oxide that masks the silicon from doping during the diffusion (predeposition) operation itself, but also the thickness that will mask during subsequent heat treatments. Thus, according to [18], a silicon oxide thickness of about 0.3 \( \mu \)m completely masks silicon during phosphorus diffusion lasting 30 minutes at \( T = 1323 \) K, but given that the predeposition operation is followed by a high-temperature phosphorus driving-in and boron diffusion operation, respectively, to take into account this duration of thermal operations, a masking coating thickness of 0.6 - 0.7 \( \mu \)m should be used.

Another mechanism for the formation of inversion layers is the diffusion of boron from silicon into SiO\(_2\) during heat treatment due to the fact that the boron segregation coefficient is below one [19]. Accordingly, with an increase in the duration of heat treatment, the degree of depletion of the silicon surface with boron increases and an inverted type of conductivity is observed.

B) Investigation of the insulation resistance between the active elements of photodiodes isolated using sections of a non-conductive substrate and a dielectric layer.

In the manufacture of PD1 samples, a decrease in insulation resistance was observed as the technological route was followed. Thus, in the trial batch of samples, the \( R_{\text{con}} \) after phosphorus diffusion, after boron diffusion, and after the metallization operation on the final crystals was monitored. After phosphorus diffusion, the \( R_{\text{con}} \) reached 10-25 M\( \Omega \). After boron diffusion \( R_{\text{con}} \approx 3-6.5 \) M\( \Omega \), and after the metallization operation \( R_{\text{con}} \approx 1.3-2 \) M\( \Omega \). The described phenomenon of
insulation resistance degradation between the REs and the GR is clearly explained by the above mechanisms of inversion layer formation. The degree of degradation can be reduced by reducing the duration of thermal operations (if possible). It should be noted that the decrease in $R_{\text{con}}$ during Cr-Au sputtering operations is caused by heating the substrates to a temperature of 473-523 K.

It is worth noting that during the storage of unsealed PD crystals for a long time, a decrease in the insulation resistance between the REs and the GR is observed. Thus, storage of crystals for about 6 months leads to a 10-30-fold degradation of $R_{\text{con}}$. This is caused by the diffusion of impurities at room temperatures.

It was also decided to investigate the actual effect of the thickness of the masking SiO$_2$ on the insulation resistance value. No change in $R_{\text{con}}$ was observed when the thickness of the oxide was alternately reduced in the gaps between the REs and the GR of the final crystals. This confirms the fact that conductivity is formed at the interface between the two phases. Also, samples of PDs with different initial thicknesses of the masking coating were fabricated by changing the duration of thermal oxidation. The oxidation operation was carried out separately, and all other operations were carried out in a single technological cycle. Half of the batches had a masking coating thickness of 0.47 μm, and the other half had a thickness of 0.61 μm. By controlling the values of $R_{\text{con}}$ after phosphorus diffusion, it was seen that samples with a smaller oxide film thickness had $R_{\text{con}} \approx 5.4 - 5.8$ MΩ, and samples with a larger oxide thickness had $R_{\text{con}} \approx 8 - 10$ MΩ. On the final crystals, samples with a smaller oxide thickness had $R_{\text{con}} \approx 0.9 - 1.1$ MΩ, and those with a larger one had $R_{\text{con}} \approx 2 - 2.5$ MΩ. It can be seen from this that a decrease in the thickness of the masking coating with a significant overall duration of thermal operations can lead to a decrease in the insulation resistance between the active elements of photodetectors according to the mechanisms described above. However, it should be noted that the values of dark currents of the PDs in the case of a shorter thermal oxidation operation are two times lower than in the case of a longer oxidation. This is probably due to a decrease in the amount of uncontrolled impurities introduced into the semiconductor volume during the high-temperature operation.

It should be noted that in the presence of inversion layers at the interface between the two phases, it is possible to increase the values of the dark currents of the guard rings ($I_{\text{GR}}$) and responsive elements, but the latter react when the insulation resistance is reduced to tens of kilohms, and the GRs react even with a slight decrease in $R_{\text{con}}$. Thus, a graph of the dependence of the dark current of the guard rings on the voltage at different values of $R_{\text{con}}$ was obtained (Fig. 7).

![Figure 7. $I$-$V$ characteristic of PD1 at different values of $R_{\text{con}}$](image)

As can be seen from Fig. 7, when the insulation resistance between the active elements decreases, the degree of increase in the $I_{\text{GR}}$ increases with an increase in the bias voltage. When testing the PDs at elevated temperatures, the increase in the dark currents of the guard rings is more pronounced and can manifest itself in the instability of the current values in time, i.e., an uncontrolled increase in $I_{\text{GR}}$ is observed without an increase in bias voltage or temperature [20].

If reduced insulation resistance values are detected after the phosphorus diffusion stage, it is necessary to completely etch the masking and anti-reflective coating in hydrofluoric acid and repeat the phosphorus driving-in operation. This will remove the oxide with the inversion layers and form a new anti-reflective coating. However, we note that this manipulation allows us to correct only those samples in which the diffusion of impurities has occurred only to the interface between the two phases. In the case of doping the silicon surface through the masking oxide, it is worth etching the surface layers by chemical-dynamic polishing [16] or plasma chemical etching [21] method, but given that the $p$-$n$-junctions have already been formed at this stage of manufacturing, these operations are complicated.

To assess the degree of undesirable doping of the silicon surface by measuring $R_{\text{con}}$ before and after oxide etching, a study was conducted: the entire oxide film was removed from a PD crystal with $R_{\text{con}} \approx 133$ kΩ and a value of $R_{\text{con}} \approx 157$ kΩ was obtained. In this case, there was no significant increase in the insulation resistance after removing the oxide, indicating the presence of conductive channels on the silicon surface due to donor doping. Another case was also observed during the study: the entire oxide film was removed from the PD crystal with $R_{\text{con}} \approx 3.3$ kΩ and a value of $R_{\text{con}} \approx 10$ MΩ was obtained. This indicated that the conductive channels were formed at the Si-SiO$_2$ interface, but
the impurities did not diffuse into the silicon surface. Accordingly, in the second case, it is possible to repeat the phosphorus driving-in operation with positive results, and samples as in the first case can be restored only after a shallow etching of the plate surface. It is worth noting that the above study shows that the predominant mechanism of inversion channel formation is the redistribution of impurities in the oxide film. It should be added that the mechanism of formation of inversion layers due to the diffusion of boron into the SiO$_2$ is more effective at a significant duration of heat treatment.

Using the described method of isolation allows obtaining an isolation resistance of 1-10 MΩ, and it should be used in photodetectors with a relatively low bias voltage. When using silicon with $p\geq 20$ kΩ, this method is ineffective.

C) Investigation of the insulation resistance between the active elements of photodiodes isolated using mesa-profile grooves with a dielectric film

It is possible to increase the value of insulation resistance relative to PD$_1$ by using a crystal topology with a mesa profile. In the case of manufacturing samples using the PD$_2$ technology, it is possible to obtain $R_{\text{con}} \approx 13$-16 MΩ. The reason for the increase in insulation resistance between the active elements is the absence of an oxidation operation (no masking SiO$_2$) and a reduction in the total duration of thermal heating. In this case, the stage of formation of the anti-reflective oxide is followed by only one thermal operation - boron diffusion, which is low-temperature relative to the previous thermal operations. During boron diffusion, the probability of diffusion of uncontrolled impurities through the oxide is minimal. It is worth noting that an important factor in the increase in the $R_{\text{con}}$ of PD$_2$ is the absence of phosphorus diffusion through the masking oxide windows, since the diffusion was carried out before the formation of anti-reflective SiO$_2$, respectively, in this case there is no phenomenon of diffusion of phosphorus in the oxide to the surface of silicon during heat treatment.

Given that one of the factors of inversion channels formation is the diffusion of impurities from the masking oxide into the substrate, it is necessary to reduce the width of the gaps between the elements. Therefore, the question arises whether the masking coating cannot be removed after it has performed its functions, i.e. after the phosphorus predeposition operation. In this case, the anti-reflective oxide grown during the phosphorus driving-in will be a protective layer on the front side of the substrate during the diffusion of boron to the back side. To confirm or refute this statement, the experiment described above was carried out. Measuring the resistance of insulation between the REs and GR of final crystal, it was seen that serial samples had $R_{\text{con}} \approx 4$-5.7 MΩ, and samples with masking oxide etched before phosphorus driving-in had $R_{\text{con}} \approx 0.6$-1 MΩ. The experiment showed that the etching of the masking oxide after phosphorus predeposition is negative, but in the case of samples with mesostructures, the presence of only an anti-reflective coating contributes to an increase in $R_{\text{con}}$. Nevertheless, it should be borne in mind that PD$_2$ has one less high-temperature operation in the technological route than PD$_1$. Although the described assumptions require additional research.

D) Investigation of the insulation resistance between the active elements of photodiodes isolated using surface leakage restriction channels isotopic with the substrate material

Isolation of active photodiode elements by means of $p$-type regions in the gaps between the elements allows to obtain the highest values of insulation resistance. The formation of these regions with a width of 100 μm in the gaps with a width of 200 μm allowed us to obtain $R_{\text{con}} = 25$-30 MΩ. It should be noted that the implementation of this method of isolation requires the introduction of two additional thermal operations - boron diffusion to the front side of the substrate and boron oxidation/driving-in of boron. This factor can contribute to an increase in dark currents and a decrease in responsibility due to the degradation of the lifetime of non-basic charge carriers and the resistivity of the material due to an increase in the total duration of thermal operations [1]. In order to avoid the above, it is worthwhile to carry out gettering of generation and recombination center operations with modes that allow restoring the above parameters [22].

It is worth noting that the PD$_3$ technological route can be shortened. For example, it is possible to diffuse boron simultaneously to the front side to form areas of leakage channel confinement and to the back side of the substrate to form an ohmic contact. However, in this case, there is a need to include additional operations to ensure masking of the $p^-$-type areas on the front side, which will be without a masking coating after the boron diffusion operation.

By introducing the boron diffusion operation into the entire area of the substrate front side with a low concentration (the first thermal operation), it is possible to avoid the need for additional photolithography or operations to form masking coatings. The key aspect of this method is the low concentration of diffused boron, since with an increase in the impurity concentration, the PD may fail due to an avalanche-like increase in dark currents, since in this case the crystal structure will resemble an avalanche photodiode [23]. Low concentrations can be achieved by lowering the temperature or duration of the operation, and the most effective method is ion implantation. Thus, when the entire surface of the substrate was doped with boron with a surface resistance of $R_s = 175$-200 Ω cm, it was possible to obtain $R_{\text{con}} = 40$ MΩ on the final samples.

It should be noted that the introduction of a boron impurity into the substrate surface reduces the density of dislocations formed during phosphorus diffusion. Since dislocations are formed during phosphorus diffusion due to the mismatch of the radius of phosphorus and silicon atoms: phosphorus atoms are larger than silicon atoms, mechanical stresses arise due to this difference, which leads to the formation of structural defects [24]. And since the radius of boron atoms is smaller than that of silicon, this will compensate for mechanical stresses and reduce the probability of dislocation formation due to the described mechanism.

The method of isolation by $p^-$-regions should be used at $p \geq 20$ kΩ cm, when using high bias voltages and when it is necessary to reduce the width of the gaps between the Res.
CONCLUSIONS

A comparative analysis of three methods of isolation was carried out: classical – isolation with the surface of a conditionally non-conductive substrate and a dielectric layer (PD1); insulation using mesa-profile grooves with a dielectric film (PD2); and isolation using surface leakage restriction channels isotypic with the substrate material (in this case p'-type) formed in the gaps between the active element (PD3). The following conclusions were made during the research:
1. The reason for the degradation of the insulation resistance between the active elements of photodiodes is the presence of conductive inversion channels at the interface Si-SiO₂.
2. One of the mechanisms for the formation of conductive inversion channels at the Si-SiO₂ interface and the reduction of insulation resistance between active elements is the redistribution of impurities in the masking oxide (including phosphorus) and their diffusion to the interface of the two phases during thermal operations. Another mechanism for the formation of inversion layers is the diffusion of boron from silicon into SiO₂ during heat treatment due to the fact that the boron segregation coefficient is below one.
3. In the manufacture of PD3 samples, a decrease in insulation resistance was observed as the technological route was followed. The degree of degradation can be reduced by reducing the duration of thermal operations.
4. Reducing the thickness of the masking oxide causes a decrease in insulation resistance.
5. If reduced insulation resistance values are detected after the phosphorus diffusion stage, it is necessary to completely etch the masking and anti-reflective coating in hydrofluoric acid and repeat the phosphorus driving-in operation.
6. In the case of manufacturing samples using the PD2 technology, it is possible to obtain $R_{con} = 13-16 \, \text{M} \Omega$. The reason for the increase in insulation resistance between the active elements is the absence of an oxidation operation (no masking SiO₂) and a reduction in the total duration of thermal heating.
7. Isolation of photodiode elements by means of p'-type regions in the gaps between the elements allows to obtain the highest values of insulation resistance. The formation of these regions with a width of 100 μm in the gaps with a width of 200 μm allowed us to obtain $R_{con} = 25-30 \, \text{M} \Omega$.
8. When the entire surface of the substrate was doped with boron with a surface resistance of $R_s = 175-200 \, \Omega$, it was possible to obtain $R_{con} = 40 \, \text{M} \Omega$ on the final samples. Introduction of a boron impurity into the substrate surface reduces the density of dislocations formed during phosphorus diffusion.

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слова після (та ізоляція підкладки, допомогою що термообробок власне: класичних оптимальних кожного ізоляції опір що погіршення плівкою методів ізоляції підкладки ізоляція областей, активні й ізоляції підкладки (в даному випадку p⁺-типу), утворених у зазорах між активними елементами. Під час досліджень встановлено, що причиною погіршення опору ізоляції між активними елементами фотодіодів є наявність провідних інверсійних каналів на межі розділу Si-SiO₂ внаслідок використання кремнію із високим питомим опором. Одним із механізмів утворення інверсійних каналів є перерозподіл домішок у маскувочому оксиді (зокрема фосфору) та їх дифузія до межі розділу двох фаз під час термічних операцій. Іншим механізмом утворення інверсійних шарів є дифузія бору з кремнію в SiO₂ під час термообробок через те, що коефіцієнт сегрегації бору менше одиниці. При виготовленні зразків з ізоляцією за допомогою непровідних ділянок підкладки спостерігалося зниження опору ізоляції по мірі виконання технологічного маршруту (після кожної наступної операції опір деградував). Ступінь деградації можна знайти за рахунок скорочення тривалості термічних операцій. Побачено, що зменшення товщини маскувочого оксиду викликає зниження опору ізоляції. При використанні меза-технології вдається підвищити опір ізоляції за рахунок виключення високотемпературної операції окислення та власне завдяки відсутності маскувочого покриття під час загонки фосфору. Ізоляція активних елементів фотодіодів за допомогою ділянок p⁺-типу в проміжках між елементами дозволяє отримати найвищий значення опору ізоляції. Формування цих областей шириною 100 мкм у зазорах ширинною 200 мкм дозволило отримати опір ізоляції 25-30 МОм. Для забезпечення ізоляції активних елементів фотодіодів даним методом в технологічній маршрут вноситься дві додаткові термічні операції. Скороти кількість термічних операцій можна легуванням всієї поверхні кремнію низькою концентрацією бору перед утворенням маскувочого покриття.

Ключові слова: кремній; фотодіод; опір ізоляції; оксид кремнію; інверсійний шар