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PROBLEMS OF MASKING AND ANTI-REFLECTIVE SiO_2 IN SILICON TECHNOLOGY[†]

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The article examines the problems of thermal oxidation of silicon. Oxidation plays an important role in planar technology, which in turn is the basis of the technology of silicon integrated circuits, photodetectors and other solid-state electronics. During our production of silicon *p-i-n* photodiodes, a number of systematic types of defects and deterioration of product parameters caused by the degradation of masking or anti-reflective coatings during the manufacturing process were observed. A decrease in the insulation resistance of responsive elements in multi-element photodiodes was observed, which contributed to the increase of dark currents. A decrease in the responsivity of the products due to the degradation of the thickness or structure of the anti-reflective coating during technological operations, etc., was also revealed. It was established that the reason for the decrease in insulation resistance is the formation of inversion layers at the Si-SiO_2 interface, the presence of which can be detected when measuring *CV*-characteristics. It was also established that chemical treatment of substrates with SiO_2 in boiling acid solutions helps to reduce the thickness of the oxide. To avoid deviation of the thickness of the film from the condition of minimum reflection, it is necessary to grow a thicker layer of anti-reflective coating. It is noted that when etching the oxide during photolithography or when removing the PSG/BSG in hydrofluoric acid, it is not permissible to remove the cassette with plates from the solution for a long time, as this leads to uneven etching of the film due to the flow of the herb on the surface of the substrate. The causes of defect formation in Si and SiO_2 during oxidation are given. Thus, with improper mechanical and chemical processing of the plates, cristobalite inclusions may form in the film during oxidation. Cristobalite has a higher density than quartz glass, and the boundaries between amorphous regions and denser crystalline regions represent voids, which can be filled both by impurities from the surface and by the diffusant in the diffusion process. Also, during oxidation in silicon, packing defects are often formed. Centers of defect genesis can be mechanical damage to the plate surface or growth defects.
Keywords: *silicon; photodiode; oxidation; silicon oxide; volt-farad characteristic; transparent film*
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Oxidation plays an important role in planar technology, which in turn is the basis of the technology of silicon integrated circuits, photodetectors and other solid-state electronics [1]. At the initial stages of the development of planar technology, oxidation was used only for the manufacture of masking coatings that prevented the penetration of impurities into certain areas of the crystals during diffusion, as well as for the creation of a protective passivating layer after the device was manufactured. Recently, SiO_2 began to be used as active and passive elements in silicon functional blocks [2], as well as anti-reflective coatings (ARC) in photoreceiving devices [3]; this led to a new intensive study, it would seem, of the oxidation process and the properties of the oxide layer. In particular, conditions for the growth of nanometer films of silicon oxide are actively studied and modeled, which is relevant for miniaturization and increasing the speed of electronic elements [4, 5].

To date, a large number of methods have been developed, which have become standard, and allow obtaining high-quality oxide films, in particular, uniform in thickness, perfect in structure, and possessing high insulating properties. To a greater extent, these methods were developed empirically and are based on various processes: from thermal or anodic oxidation to deposition of a film from an external source [6]. Of course, to obtain oxide films with specified electrical properties, it is necessary to strictly control the behavior of impurities in the process of film formation, which is an urgent scientific and technical task.

During our production of silicon *p-i-n* photodiodes (PDs), a number of systematic types of defects and deterioration of product parameters caused by the degradation of masking or anti-reflective coatings during the manufacturing process were observed. A decrease in the insulation resistance of responsive elements (RE) in multi-element PDs was observed, which contributed to the increase of dark currents (I_d). A decrease in the responsivity of products (S_{pulse}) due to the degradation of the thickness or structure of the ARC during technological operations, etc., was also revealed. The described types of defects required a detailed study to establish the causes of their occurrence and methods of their avoidance.

When reviewing literary sources, it is seen that many works are devoted to the electrical properties of SiO_2. In particular, in a number of studies, the deterioration of the reverse characteristics is associated with the presence of positive fixed or mobile charges in the oxide film [7, 8]. Thus, a quantitative model of the formation of a fixed charge in silicon dioxide during thermal oxidation was developed in [7]. It was established that the amount of charge determines the number of internodal silicon atoms near the Si-SiO_2 interface, and an increase in the oxidation temperature contributes to a decrease in the value of the fixed charge due to an increase in the diffusion coefficient of internodal silicon atoms in SiO_2.

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In [8], the effect of isothermal annealing in an inert atmosphere of structures with silicon oxide was investigated, and it was established that annealing allows reducing the amount of charge in the oxide. Note that in the case of silicon *p-i-n* PDs technology (and other electronic elements) there is no possibility of increasing the oxidation temperature due to the increase in the rate of degradation of the resistivity of the original material (ρ) and the life time of minor charge carriers (τ) [9]. This degradation is caused by an increase in the diffusion coefficients of the ions of uncontrolled impurities (Li^+, Na^+, K^+), which diffuse into the substrate during oxidation (which can also be the reason for the increase in the amount of mobile charge). It is worth noting that metals contribute to the amount of charge by changing (disrupting) the structure of the oxide. For the same reason, there is no possibility of introducing additional thermal operations into the technological production routes for annealing, as well as to avoid an increase in the number of thermal shocks.

Information about the degradation of oxide films and the influence of these factors on the responsivity of the PDs was not found in the literature. There are also no technological recommendations for avoiding the degradation of the insulation resistance of REs in multi-elements PDs. Accordingly, the study of the causes of the appearance and methods of avoiding the degradation of the masking and anti-reflective oxide films in the technology of silicon *p-i-n* PDs is the purpose of this work.

EXPERIMENTAL

The research was carried out on silicon four-element *p-i-n* PDs with a guard ring (GR) designed to detect radiation with a wavelength of λ=1064 nm. The production was carried out by diffusion-planar technology according to the technological regimes given in [10]. The starting material was single-crystal dislocation-free p-type silicon with orientation [111], ρ≈18-22 kΩ·cm and τ≈1.8-2.2 ms. The technological process consisted of a complex of thermal operations and photolithography: semiconductor substrates were oxidized; photolithography was carried out to create windows for phosphorus diffusion; diffusion of phosphorus (predeposition) to the front side to create n^+-type REs and GR; drive-in of phosphorus in an oxygen atmosphere to redistribute the alloying impurity, increase the depth of the n^+-p-transition and form a anti-reflective coating; diffusion of boron to the reverse side of the substrate to create a p^+-type ohmic contact; photolithography for creating contact windows; sputtering of Cr-Au on the front and back sides.

Masking SiO_2 was formed during the first thermal operation at a temperature of T=1423 K according to the principle of dry-wet-dry oxidation [5]. Considering that the thickness of silicon oxide, which completely masks from the long-term diffusion of phosphorus at T=1323 K, reaches 0.3-0.4 μm [11], the thickness of the masking SiO_2 reached d_{SiO2}≈0.6-0.7 μm. This thickness is also chosen taking into account the redistribution of phosphorus in the oxide during subsequent thermal operations.

Anti-reflective silicon oxide was formed during the drive-in of phosphorus in an atmosphere of dry oxygen at a temperature of T=1423 K. The thickness of SiO_2 was 0.18-0.19 μm, which corresponds to the minimum reflection condition [12]:

$$\frac{\lambda}{4} = nd_{SiO_2} \tag{4}$$

where λ is the working wavelength; n the refractive index of SiO_2; d_{SiO_2} is the thickness of the anti-reflective film.

To study the structural perfection of the surface of the substrates after thermal operations, selective etching was carried out in Sirtle's etchant [13].

After oxidation and each subsequent thermal operation, the high-frequency volt-farad (*CV*) characteristics of the metal-oxide-semiconductor-structures (MOS) were measured at a frequency of 30 kHz, which made it possible to predict the final parameters of the products.

The level of pulsed monochromatic sensitivity of PDs was determined at λ=1064 nm, bias voltage U_{bias}=120 V and pulse duration τ_i=500 ns.

An important parameter of multi-element PDs with GR is the resistance of the isolation of the REs between themselves and the insulation resistance of the REs and the GR, the decrease of which leads to an increase in the photocoupling coefficient and dark currents. Determination of insulation resistance of REs and GR (R_{con}) was carried out according to the method given in [14] with U_{bias}=2 V and load resistance R_l=10 kΩ.

The thickness of the oxide films was measured by the ellipsometric method.

RESULTS OF THE RESEARCH AND THEIR DISCUSSION

A) Study of *CV*-characteristics

Measuring the *CV* characteristics of MOS structures at the initial stages of manufacturing makes it possible to estimate the final parameters of the products. Thus, in the case of *p-i-n* PDs manufacturing, the technological route consisted of 4 thermal operations, after each of which (except for phosphorus predeposition) *CV*-characteristics were measured. From the volt-farad characteristics, it is possible to determine the charge level in the oxide and detect the presence of inversion layers (IL) at the Si-SiO_2 interface. A typical *CV*-characteristic of the MOS structure for *p*-type silicon is shown in Fig. 1 (curve 1). When the number of charged states at the interface of two phases increases, the curve may shift to the left relative to the ordinate axis. As mentioned above, this leads to an increase in dark currents. But sometimes the formation of inversion layers at the Si-SiO_2 interface is observed, which form surface conductive leakage channels and reduce the insulation resistance between the REs.

The formation of ILs is possible both during the formation of a masking coating and during subsequent thermal operations. On Fig. 1 shows typical curves of volt-farad characteristics of MOS structures with inversion layers (curves 2-4). Curve 3 describes the case of doping of the silicon surface with uncontrolled impurities during oxidation, which led to a change in the conductivity type of the silicon surface to the opposite. Such a case is also possible in the presence of hydrochloric acid residues after purging quartz reactors for the purpose of cleaning from alkali metals. Curves 2 and 4 describe the case of the formation of inversion layers during the phosphorus dispersal and boron diffusion operations.

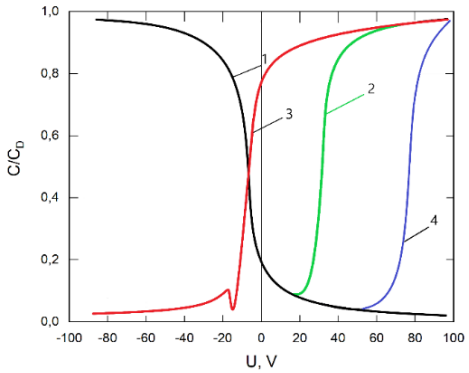


Figure 1. *CV*-characteristics of MOS structures: 1 – typical characteristic for *p*-type silicon; 2-4 – inverted characteristics

In the case of the formation of ILs during oxidation, it is necessary to etch the oxide and doing re-oxidation. The insulation resistance of REs and GR in samples with *CV*-characteristics of the Curve 2 type (Fig. 1) reached R_{con}≈1-10 kΩ at R_{con} ≈5-15 MΩ for serial PDs. And dark current of GR J_{GR}≈7-36 mA/cm^2 at J_{GR} ≈3.6-36 μA/cm^2 (U_{bias}=120 V) for serial products. It is impossible to accurately measure the REs of defective PDs, since it constantly increases due to the flow of charge carriers from the GR. It is possible to fix only the initial value, which reaches J_d≥26 μA/cm^2 at J_d = 65-130 nA/cm^2 for serial samples. In the case of SiO_2 etching and re-oxidation, a decrease in dark currents is observed, but as experiments show, after re-oxidation, the values of I_d and I_{GR} are slightly higher than in serial products. This indicates the presence of residual inversion layers on the surface of the substrate, they can be eliminated by plasma-chemical or chemical-dynamic methods.

The insulation resistance of samples with *CV*-characteristics of the Curve 4 type (Fig. 1) reached R_{con} ≈ 200-600 kΩ, and J_{GR}≈50-100 μA/cm^2. From the above, it is possible to conclude that it is possible to estimate the conductivity of surface inversion channels based on the volt-farad characteristics.

The causes of ILs are known and studied [15]. The key factor in their formation is an increase in the resistivity of the substrate, since with an increase in ρ of the material, a smaller amount of impurities is needed to change the surface conductivity to the opposite [16]. In most cases, an inversion layer is already present on *p*-type silicon with ρ=1-10 Ohm·cm [17]. In the case of a thermal oxidation operation, the possible technological reasons for the appearance of inversion are improper chemical treatment of substrates, the presence of alkali metal impurities in deionized water, quartz vessels, or a quartz reactor, and carrier gases. However, the appearance of ILs during boron diffusion is caused by the redistribution of impurities in SiO_2 and their diffusion to the Si-SiO_2 interface [18]. These impurities were introduced into the oxide during previous thermal operations and diffused into the surface layer of silicon due to the high total duration of thermal treatments. Another factor that contributes to the formation of ILs with a high total duration of thermal operations is the diffusion of boron atoms from the near-surface layers of silicon into the oxide, since the segregation coefficient of boron is below unity [19].

The probability of the appearance of inversion layers can be minimized by careful control of carrier gases, deionized water for the presence of alkali metals, and periodic purging of quartz reactors with hydrochloric acid vapors. It is possible to increase the resistance of the insulation of REs and GR by forming regions of restriction of leakage channels in the gaps between active elements of the PD isotype with the substrate material [14]. It is possible to reduce the influence of the inversion layers of the periphery of photodiode crystals on the level of dark currents of the GR when the masking oxide is etched from the periphery and new film is formed in the dry oxygen atmosphere during the operation of drive-in of phosphorus [20].

B) Reduction of the thickness of anti-reflective SiO_2 in the process of PDs manufacturing.

During the serial production of silicon *p-i-n* PDs, a decrease in the thickness of the ARC was noticed in the process of technological operations after its formation, this factor led to a decrease in responsivity, since the responsivity of the PD is directly proportional to the reflection coefficient of the anti-reflective film [21]:

$$S_\lambda = (1-R)TQ\alpha_{p-n}\frac{\lambda}{1.24} \quad (2)$$

where R is the ARCs reflection coefficient; T is the transmission coefficient of the input window or optical filter; Q is the quantum output of the internal photoeffect; α_{p-n} is the collection coefficient of minor charge carriers generated by radiation in the active region of the photodiode.

When studying what was described, it was seen that the reason for the decrease in d_{SiO2} is chemical treatment (CT). Accordingly, it was decided to study the influence of CT on the thickness of SiO_2.

To clean the substrates, we used CT in boiling solutions of acids with the composition indicated in Table 1, the treatment duration was 10 minutes. To study the change in d_{SiO2} in the process of washing before and after operations, the thickness of this coating was measured.

Table 1. The composition of acid solutions for CT of silicon substrates and the change in d_{SiO2} during the operation

Solution	Composition	Δd_{SiO2}, nm
H_2SO_4:H_2O_2:H_2O	4:1:1	6-7
HNO_3:H_2O_2:H_2O	1:1:1	8-9
NH_4OH:H_2O_2:H_2O	5:1:1	16-17

Taking into account that after the formation of the anti-reflective oxide, according to the technological route, three more 3-stage washings are carried out, which will reduce d_{SiO2} by 90-100 nm, it is necessary to increase the duration of drive-in of phosphorus, and, accordingly, the thickness of ARC.

To be able to estimate the drop in responsivity (ΔS_{pulse}) of the PD as a result of d_{SiO2} reduction, a graph of the dependence of ΔS_{pulse} on the ARC thickness was obtained (Fig. 2). The initial responsivity of the PD crystal was measured at d_{SiO2}≈0.18 μm and the oxide was digested layer by layer in a slow etchant HF: H2O=1:10. After each etching process, S_{pulse} measurements were also performed.

Reflectance spectra of PDs were obtained at d_{SiO2}≈0.170-0.175 μm and PDs without ARC (Fig. 3).

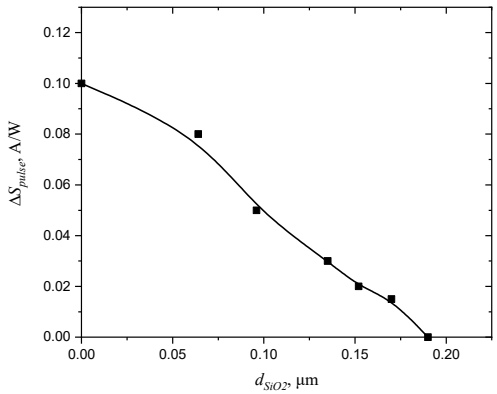


Figure 2. Experimental graph of the dependence of the drop in responsivity on the thickness of the anti-reflective coating

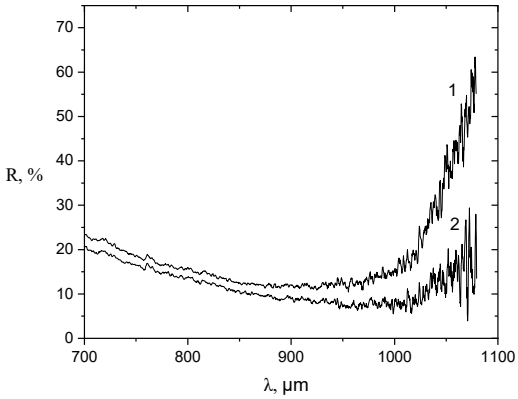
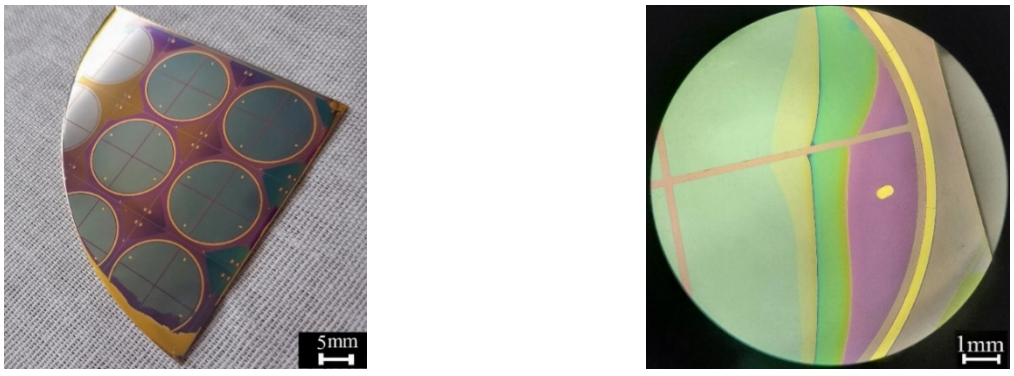


Figure 3. PDs reflection spectra: 1 - without ARC; 2 - d_{SiO2}≈0.17-0.175 μm

From Fig. 3, it can be seen that the reflection minimum of the investigated film is at λ≈1.01-1.02 μm due to the deviation of the film thickness from the optimized for λ≈1.064 μm. The reflection coefficient of PD without ARC is R≈45-50% at the working wavelength, and with a thickness of anti-reflective silicon dioxide of 0.17-0.175 μm, R≈15-20%. At d_{SiO2}=0.18-0.19 μm at λ≈1.064 μm, R=5-7%.

Changing the thickness of the masking and brightening coatings is also possible during photolithography, removal of phosphorosilicate (PSG) or borosilicate (BSG) glasses, and chemical dynamic polishing (CDP).

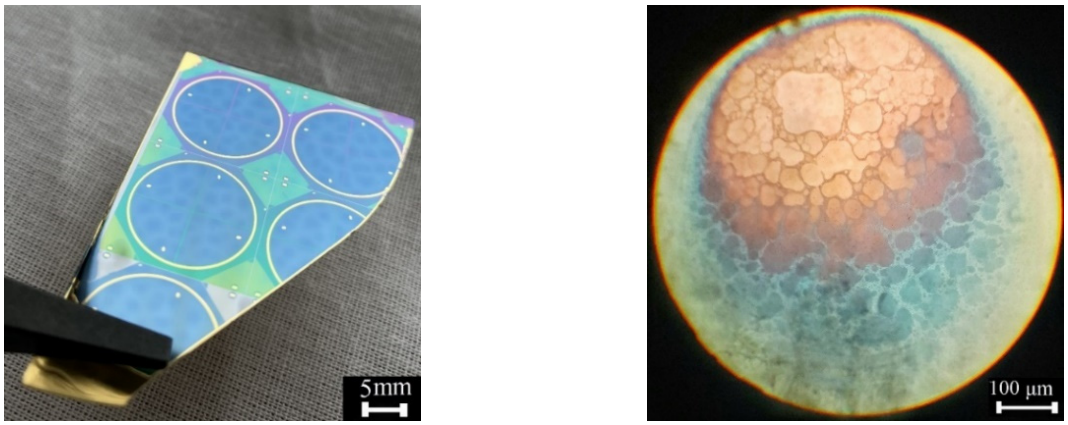
In particular, when etching the oxide during photolithography or when removing PSG/BSG in hydrofluoric acid, it is not permissible to remove the cassette with plates from the solution for a long time, as this leads to uneven etching of the surface (Fig. 4) due to the flow of the etchant on the surface of the substrate. Accordingly, non-uniformity of the film thickness can lead to scattered responsivity or uneven etching of the oxide during subsequent photolithography.



a) b)

Figure 4. Image of uneven thickness of masking (a) and anti-reflective (b) SiO_2

In order to carry out the CDP of the reverse side of the substrate, the front side is covered with a chemically resistant varnish [22]. If the thickness of the varnish is insufficient during drying, it is possible to form thinnings or punctures through which undesirable etching of the working surface of the crystal occurs. The consequence of thinning is spot etching of the oxide over the entire surface of the RE (Fig. 5 a), and in the case of punctures, the seepage of the etchant under the varnish and local etching of SiO_2 (Fig. 5, b) or even silicon, which can lead to a breakdown of the *p-n* junction. To avoid the described situation, it is worth applying a double layer of varnish with intermediate drying.



a) b)

Figure 5. Image of the dispersion of the thickness of the oxide film after CDP due to the thinning of the varnish (a) and punctures (b)

B) Defect formation during thermal oxidation

The most important condition for obtaining high-quality silicon oxide is the cleanliness of the plate before oxidation. The presence of impurities on the surface of silicon before oxidation or during the process of oxide growth negatively affects the uniformity of the film and the electrical properties of the interface.

On an uneven, contaminated surface, the grown or applied oxide contains inclusions of cristobalite (Fig. 6), which are undesirable in all classic cases of using oxide films of silicon technology. Cristobalite has a higher density than quartz glass, and the boundaries between amorphous regions and denser crystalline regions represent voids, which can be filled both with impurities from the surface and with a diffusant in the diffusion process [23]. A necessary condition for obtaining high-quality SiO_2 is the polishing of the surface of the substrates followed by chemical treatment. Ultrasonic cleaning is also possible.

Packing defects are often formed during oxidation in silicon [24]. The formation of these defects on the surface of the plates occurs for several reasons. The first is mechanical damage to the surface of the substrate during cutting or grinding. If such damages, for example, scratches or cutting marks, are not removed by subsequent chemical polishing, then they can become local areas of nucleation of packaging defects (Fig. 7a).

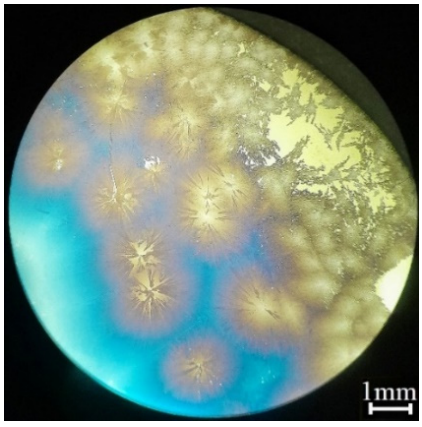
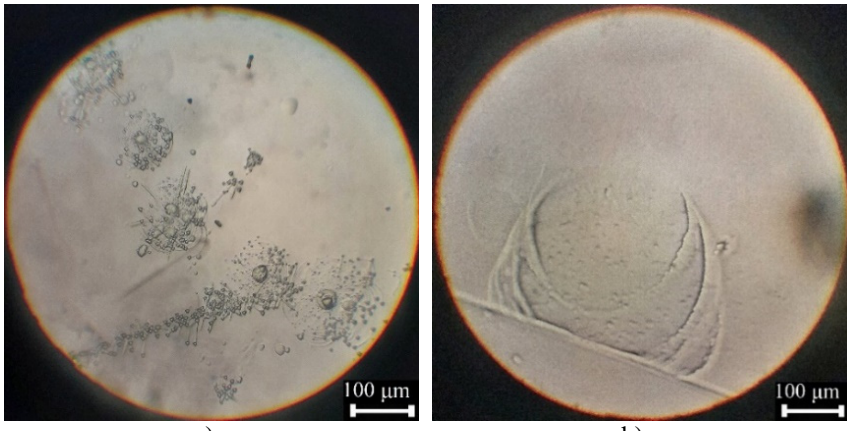


Figure 6. Image of silicon oxide with cristobalite inclusions



a) b)

Figure 7. Image of structural defects in the areas of mechanical disturbances (a) and swirl defects (b) on the surface of plates (plates after selective etching)

The second reason for the formation of packing defects (in the absence of mechanical damage on the surface) is related to the presence of growth and so-called swirl defects in the plates [25], since complexes of point defects with a swirl distribution are the seeds for packing defects during oxidation (Fig. 7b). Note that the defects formed during oxidation have an internodal nature and are associated with the accumulation and condensation of excess silicon atoms generated as a result of oxygen diffusion in silicon. It is the internodal silicon atoms that form point defect clusters in the areas of mechanical surface disturbances.

Another mechanism for the formation of structural defects during oxidation can be mechanical stresses introduced as a result of the difference in the thermal expansion coefficients of Si and SiO_2 [26]. But we did not observe the formation of defects by this mechanism.

It is worth noting that during the diffusion of phosphorus, clusters of packing defects are areas of dislocation generation. A high density of structural defects on the plate surface negatively affects the dark currents of photodiodes [27,28]. In order to avoid defect formation, it is worth using dislocation-free silicon, performing the CDP operation after mechanical processing of the wafers, and clearly controlling the substrates before thermal operations.

CONCLUSIONS

1. The problems of masking and anti-reflective SiO_2 in the technology of silicon *p-i-n* photodiodes were investigated.
2. The reason for the decrease in the insulation resistance of photosensitive elements in multi-element photodiodes is caused by the presence of surface inversion channels at the Si-SiO_2 interface. Inversion layers can be detected by measuring *CV*-characteristics.
3. Chemical treatment of oxidized substrates in boiling acid solutions helps to reduce the thickness of the oxide film.
4. When removing the cassette with oxidized plates from the solution during SiO_2, BSG or PSG etching, uneven etching of the film is possible due to the flow of the etchant on the plate.
5. Oxidation of contaminated or uneven substrates can be accompanied by the formation of oxide with the inclusion of cristobalite.
6. Defect formation during thermal oxidation occurs in areas of mechanical disturbances or growth defects.

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ПРОБЛЕМИ МАСКУЮЧОГО ТА ПРОСВІТЛЯЮЧОГО SiO_2 В КРЕМНІЄВІЙ ТЕХНОЛОГІЇ

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В статті досліджено проблематику термічного окиснення кремнію. Окиснення відіграє важливу роль в планарній технології, яка в свою чергу є основою технології кремнієвих інтегральних мікросхем, фотоприймачів та інших твердотільних засобів електроніки. При виготовленні нами кремнієвих *p-i-n* фотодіодів побачено ряд систематичних видів браку та погіршень параметрів виробів спричинених деградацією маскуючого чи просвітляючого покриттів в процесі виготовлення. Спостерігалось зниження опору ізоляції фоточутливих елементів в багатоелементних фотодіодах, що сприяло зростаню темнових струмів. Також виявлено зниження чутливості виробів внаслідок деградації товщини чи структури просвітляючого покриття під час технологічних операцій та ін. Встановлено, що причиною зниження опору ізоляції є утворення інверсійних шарів на межі розділу Si-SiO_2, наявність яких можна виявити при вимірюванні *CV*-характеристик. Також встановлено, що хімічна обробка підкладок із SiO_2 в кип'ячих розчинах кислот сприяє зменшенню товщини оксиду. Для уникнення відхилення товщини плівки від умови мінімуму відбивання варто вирощувати товстішший шар просвітляючого покриття. Зауважено, що при травленні оксиду під час фотолітографії чи при зніманні ФСС/БСС в плавиковій кислоті не припустимо виймати касету з пластинами із розчину на тривалий час, оскільки це призводить до нерівномірного травлення плівки внаслідок стікання травника по поверхні підкладки. Наведено причини дефектоутворення в Si та SiO_2 під час окиснення. Так, при неналежній механічній та хімічній обробці пластин можливе утворення включень кристобалітів в плівку під час окиснення. Кристобаліт володіє вищою густиною ніж кварцове скло, а межі між аморфними областями і більш щільними кристалічними областями представляють порожнечі, які можуть бути заповнені як забрудненнями з поверхні так і дифузантом в процесі дифузії. Також під час окиснення в кремнію часто утворюються дефекти упаковки. Центрами зародження дефектів можуть бути механічні пошкодження поверхні пластини чи ростові дефекти.

Ключові слова: *кремній; фотодіод; окиснення; оксид кремнію; вольт-фарадна характеристика; просвітляюча плівка*